

LPNHE (IN2P3 CNRS)



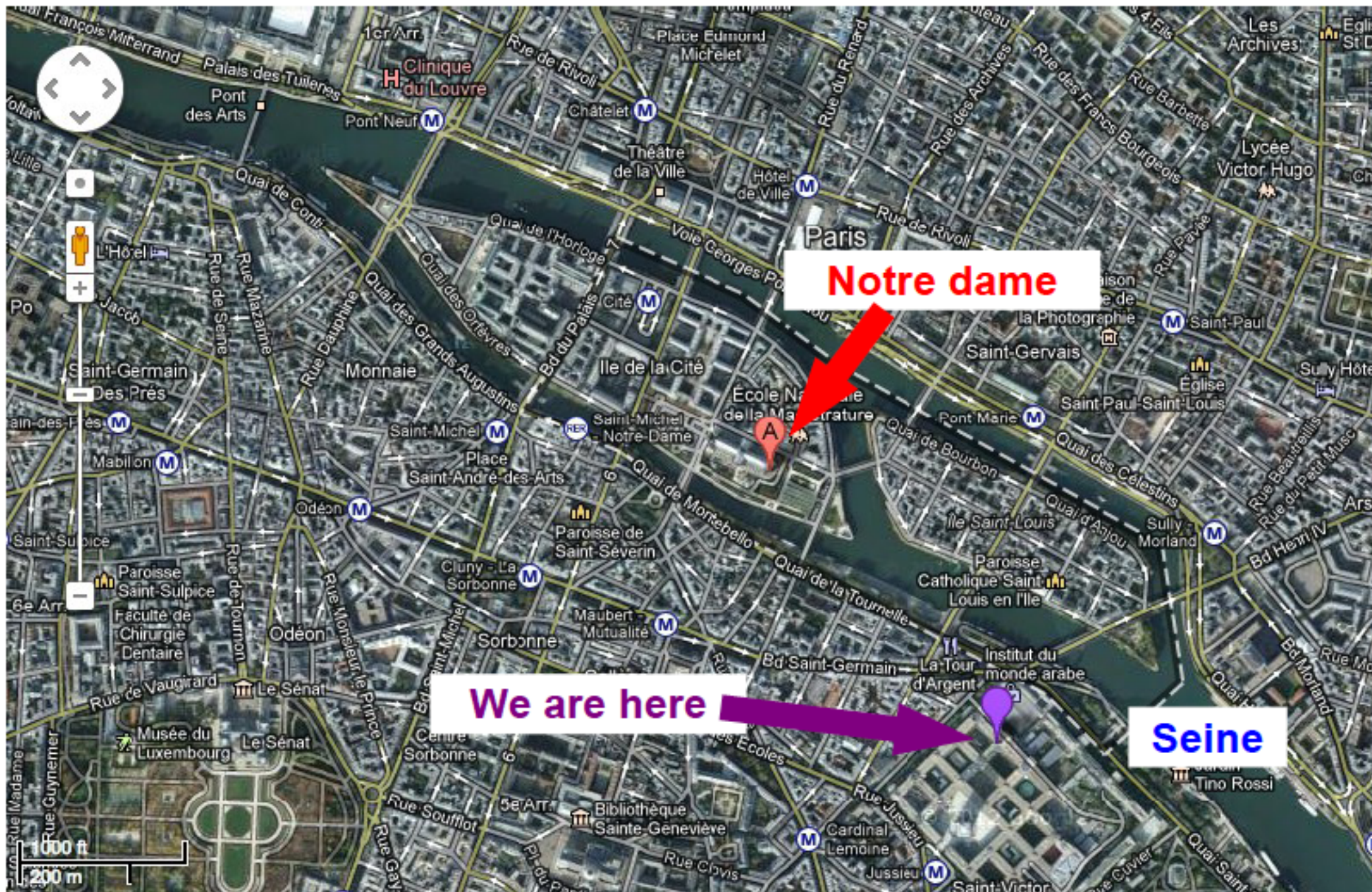
LPNHE
PARIS

Laboratoire de Physique Nucléaire et de Hautes Energies

Mixed research unit (UMR)
of Institut National de
Physique Nucléaire et de
Physique de Particules
(IN2P3 CNRS) and Pierre et
Marie Curie university
(UPMC) and Paris Diderot
university.



~ 100 researchers + 50 technical staff



LPNHE ATLAS Group

- G. Calderini (Group Leader)
- T. Beau (Staff Res.)
- M. Bomben (Post-doc)
- J. Chauveau (Prof)
- O. Davignon (PhD)
- A. Demilly (PhD)
- S. De Cecco (Staff Res.)
- F. Derue (Staff Res.)
- M.W. Krasny (Staff Res.)
- M. Kuna (Post-doc)
- D. Lacour (Staff Res.)
- B. Laforge (Prof)
- S. Laplace (Staff Res.)
- G. Lefebvre (PhD)
- B. Malaescu (Staff Res.)
- G. Marchiori (Staff Res.)
- N. Méric-Chrétien (PhD)
- I. Nikolic-Audit (Staff Res.)
- J. Ocariz (Prof)
- S. Pirès (Stage)
- C. Rangel-Smith (PhD)
- M. Ridel (Staff Res.)
- L. Roos (Staff Res.)
- Ph. Schwemling (Prof)
- T. Théveneaux-Pelzer (PhD)
- H. Torres (PhD)
- S. Trincaz-Duvoid (Staff Res)
- F. Vannucci (Prof)
- L. Yao (PhD)
- F. Crescioli
- D. Laporte
- Y. Orain,
- J.F. Genat,
- O. Ledortz
- L. Martin,
- V. Mendoza

People with implications in Si sensors and FTK

Giovanni Calderini – Director of research

in IAPP

- Former BaBar tracker project leader
- Planar pixels for ATLAS upgrade

Giovanni Marchiori – Researcher

- Experience in Silicon detectors

Marco Bomben – Post-doc

- Experience in Silicon detectors
- ATLAS pixel test beam coordinator

Jacques Chauveau – Professor UPMC

- Experience in Silicon detectors

Francesco Crescioli – Research Engineer

in IAPP

- FTK experience

Jean-Francois Genat – Research Engineer

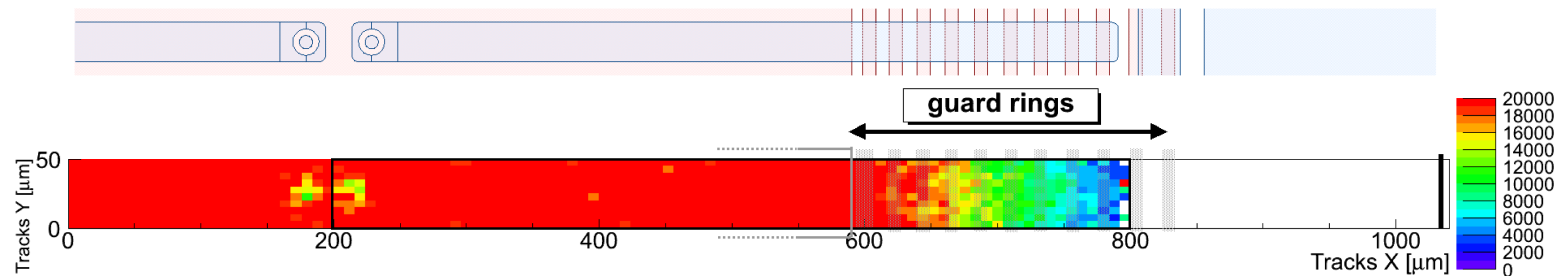
- Experience in chip design

Olivier Le Dortz – Research Engineer

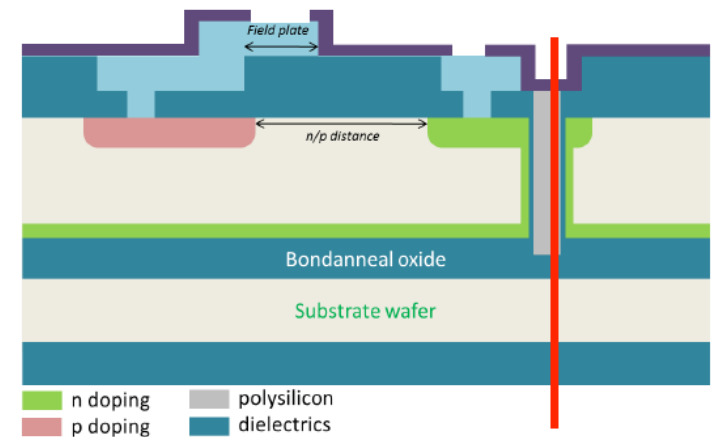
- FPGA and perif. electronics experience

Sensors

- Contribution to ATLAS IBL
 - Simulations (Silvaco)
 - pixel-over-guard rings design
 - several n-in-n and n-in-p productions



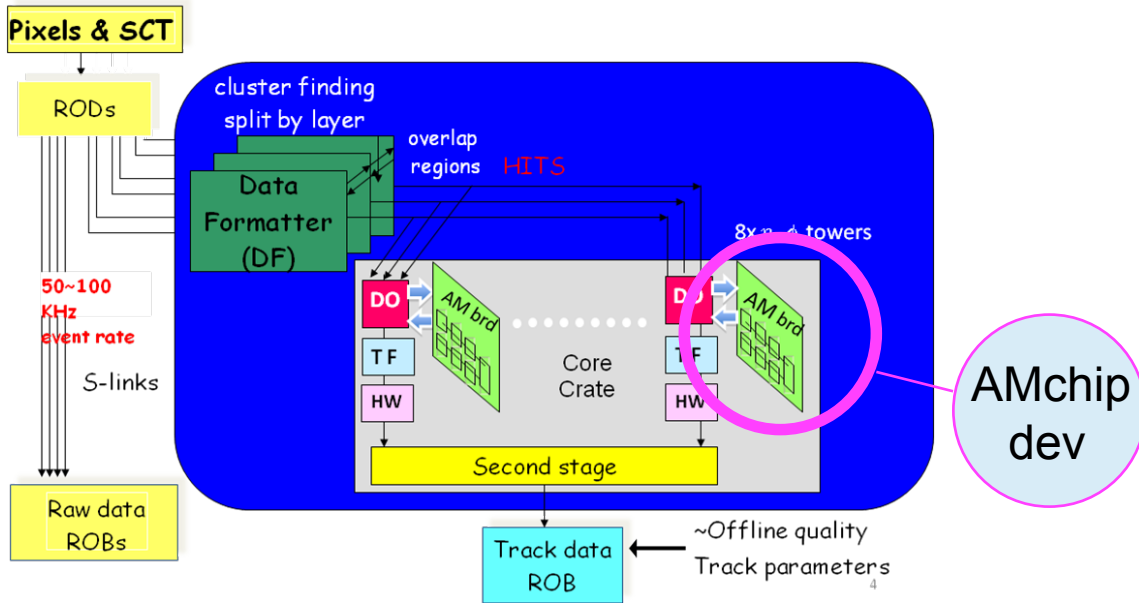
- Edgeless planar sensors (FBK-LPNHE)
 - Aim to phase-II ID (mid-outer layers)
 - Reduced dead area at periphery ($\sim 100 \mu\text{m}$)
 - Sensors designed & simulated via TCAD
 - Tests started in our clean room
 - Next: CCE at periphery w/ laser, sources, beams



Cut line

FTK experience

Hardware



Software

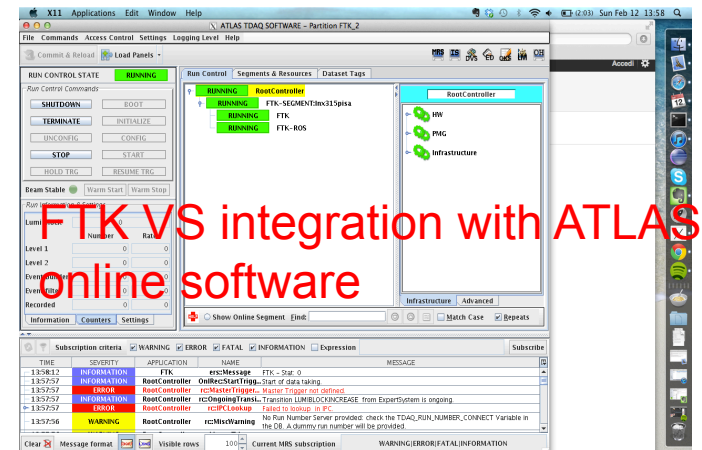
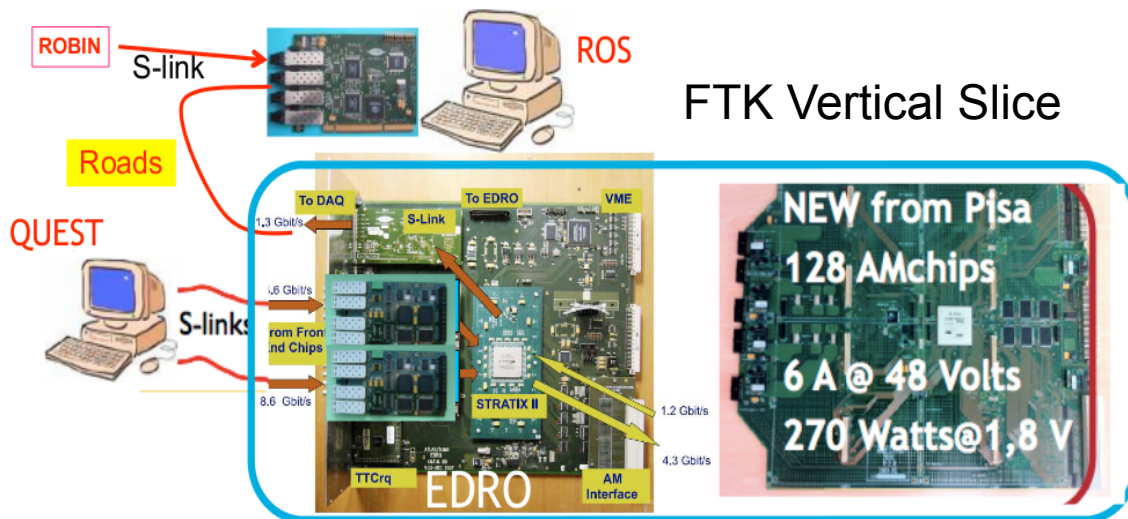
FTK simulation & data preparation software

FTKSim

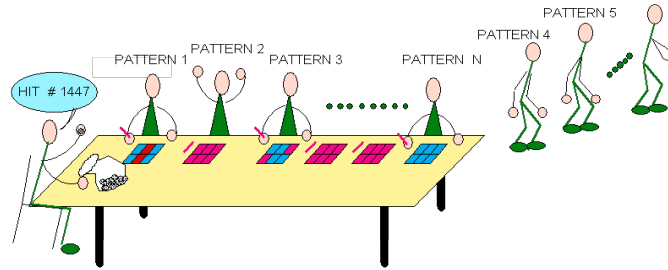
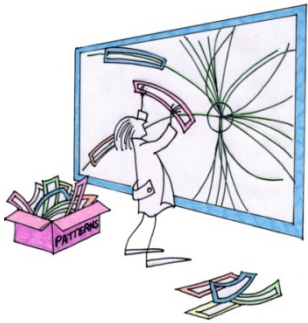
- Pattern generator from data & constants

- FTKSim in ATHENA
- JobOptions for trigger studies

FTK Vertical Slice



Associative Memory ~ AMchip



AMchip-based associative memory device first used in CDF (Amchip03).

AMchip03

- 6-layers patterns @ 18-bit
- ~5kpatt/chip
- 40 MHz

Used by
FTK VS

The associative memory is the core component of the pattern recognition stage of FTK

Performs the highly demanding task of coarse tracks finding in the full event.

The associative memory hardware is based on a custom made ASIC: AMchip

FTK needs more advanced technology:

AMchip04

- 8-layers @ 15-bit (configurable 3-7 bit w/ ternary logic)
- ~8kpatt/chip
- 100 MHz

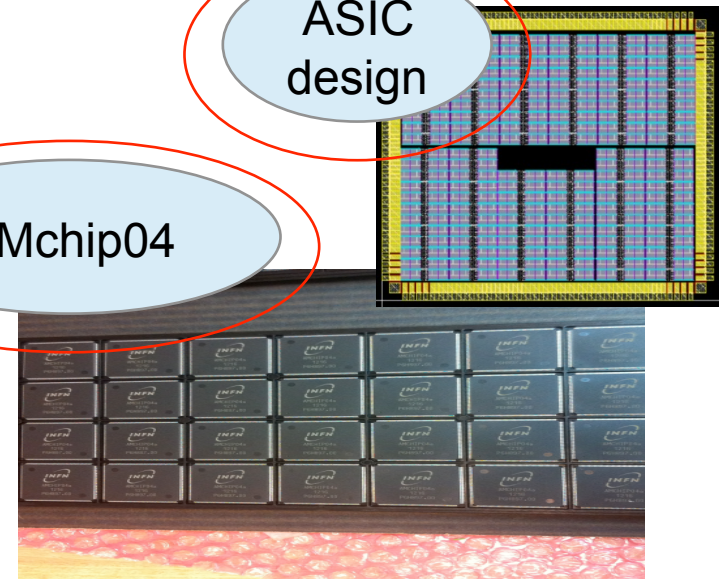
AMchip05

- High speed serial I/O
- ~32kpatt/chip
- Stream merge function

Design phase

ASIC
design

AMchip04



LPNHE activities in FTK/IAPP

- **Development of a low-noise alimentation framework for radiation damaged ATLAS sensors**
(collaboration with CAEN)
- **Test-stand development for FTK board validation and commissioning**
 - AMchip tests
 - Boards tests
 - Integration HW/SW