The Associative Memory Chip

Saverio Citraro – University of Pisa & INFN

This project has received funding from the European Union's FP7 for research, technological development and demonstration under grant agreement n 324318
FP7-PEOPLE-2012-IAPP

Outline

- The Associative Memory (AM) chip Overview
- AM chip working principles
- Internal Architecture
- Applications:
  - High Energy Physics application
  - Image Pre-Filter
  - Image Understanding
- Conclusion

AM chip overview

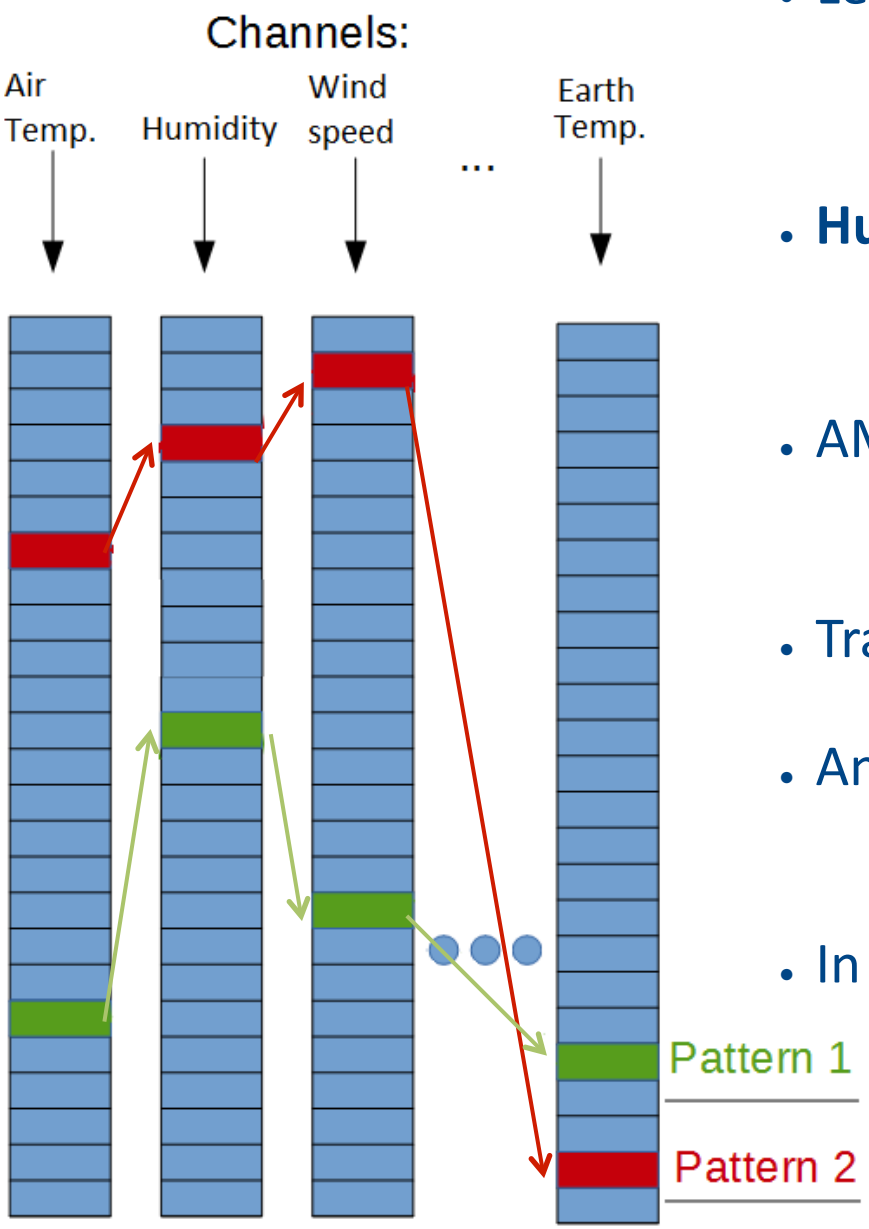
- ASIC designed by INFN
- Made of **CAM Matrix**
- AM **detects coincidences** inside large independent data streams
- Was used for High Energy Physics Experiment

  CDF at Fermilab
- Will be used for High Energy Physics Experiment

  ATLAS at CERN
- We are working to improve features

- We would like to use this Hardware for Embedded system and real time applications

How could be used?



- Let me do this Example:

  Hypothetic Situation (just to explain the idea)

- **Hundreds** of **measurements** from different sensors like thermometers, anemometers, barometers .

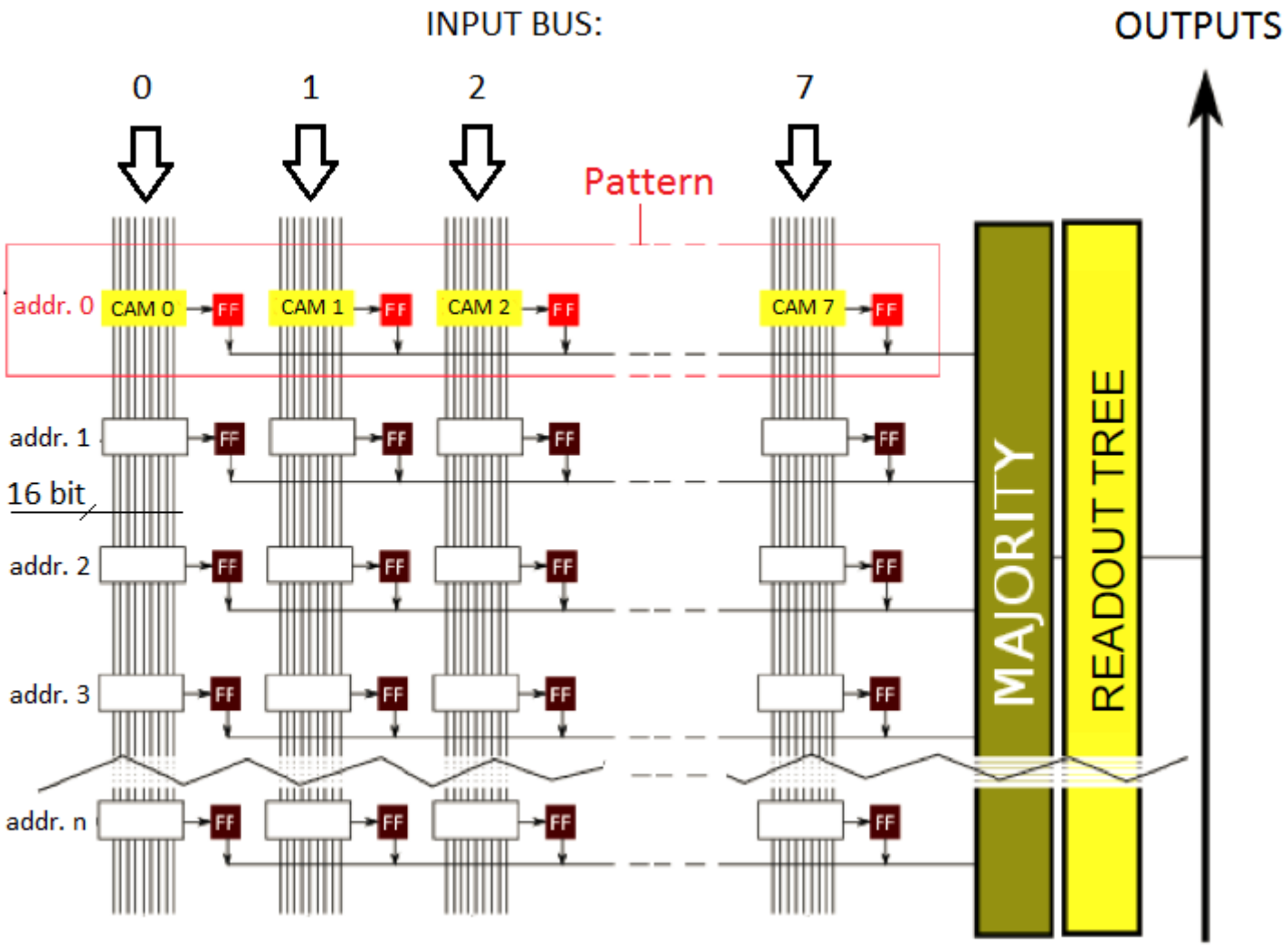
- AM searches for **coincidences** between the different input **data streams**.

- Training Phase: for a growing **tornado**.

- Analysis Phase: **Acquire data** and look the response.

- In order to **improve** the **efficiency** of the system, we can **update** the significant **data** in the **memory,** learning from the “past experience”.

Internal Architecture

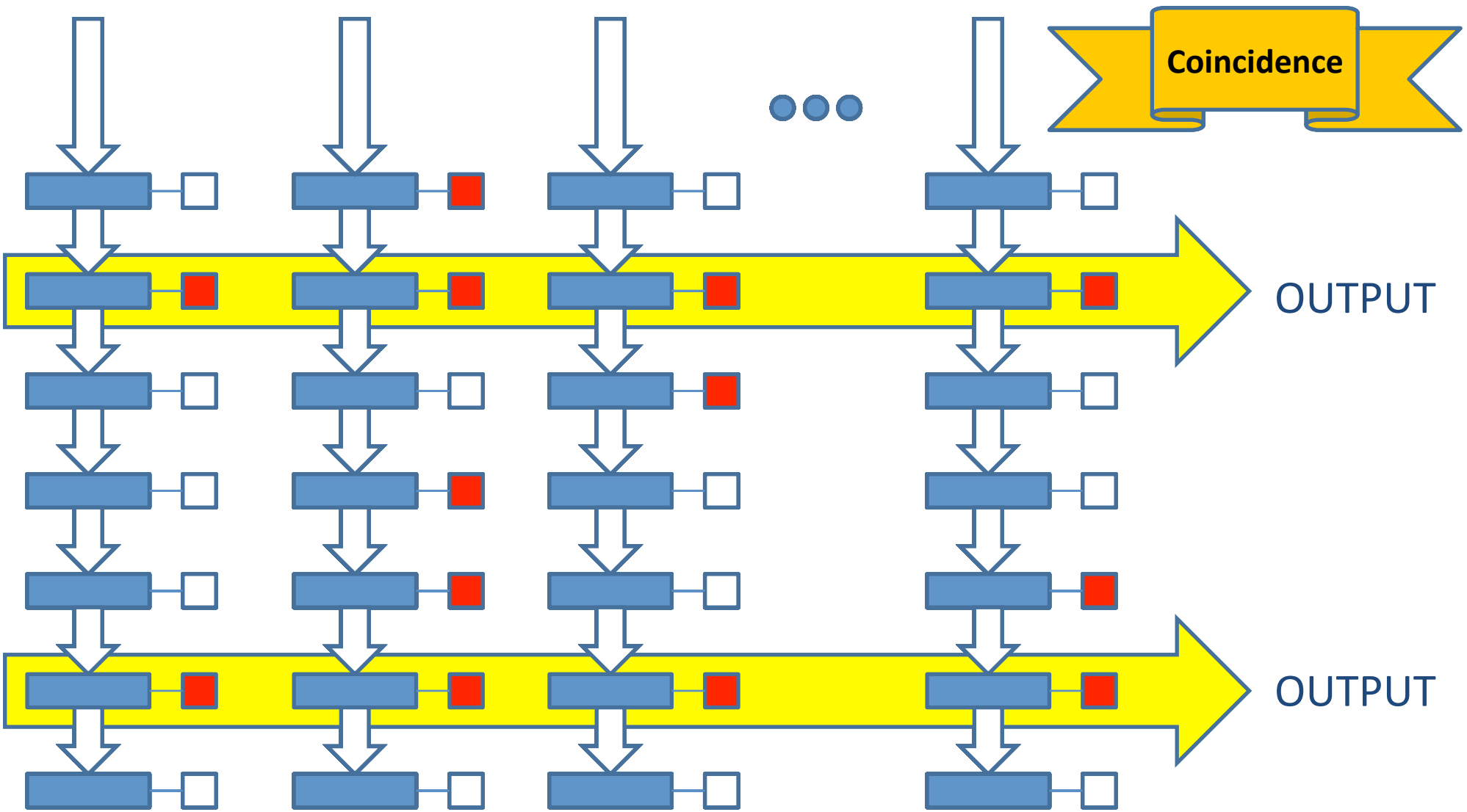


- CAM cell Matrix
- CAM cells grouped
  1 Pattern = 8 CAMs
- Each Word = 16 bit
- 128K Patterns
- Each CAM cell has a dedicate Flip-Flop
- **All CAMs** check their data with the data bus in **one clock cycle**
- Check 100 T Word/s

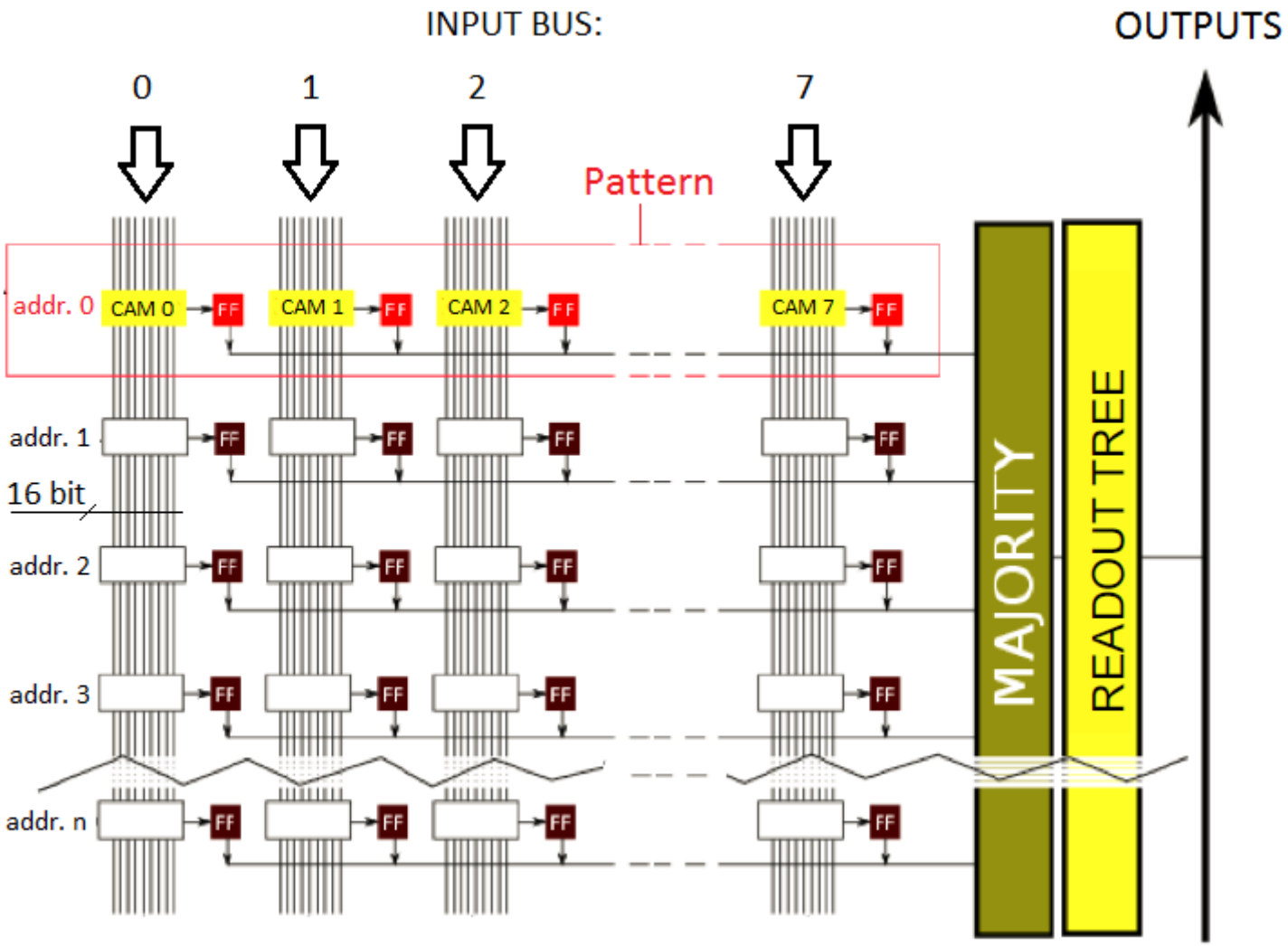
The **INPUT** buses could be **asynchronous**:

the **matches** are **independent**!

Working Example



Majority and Readout

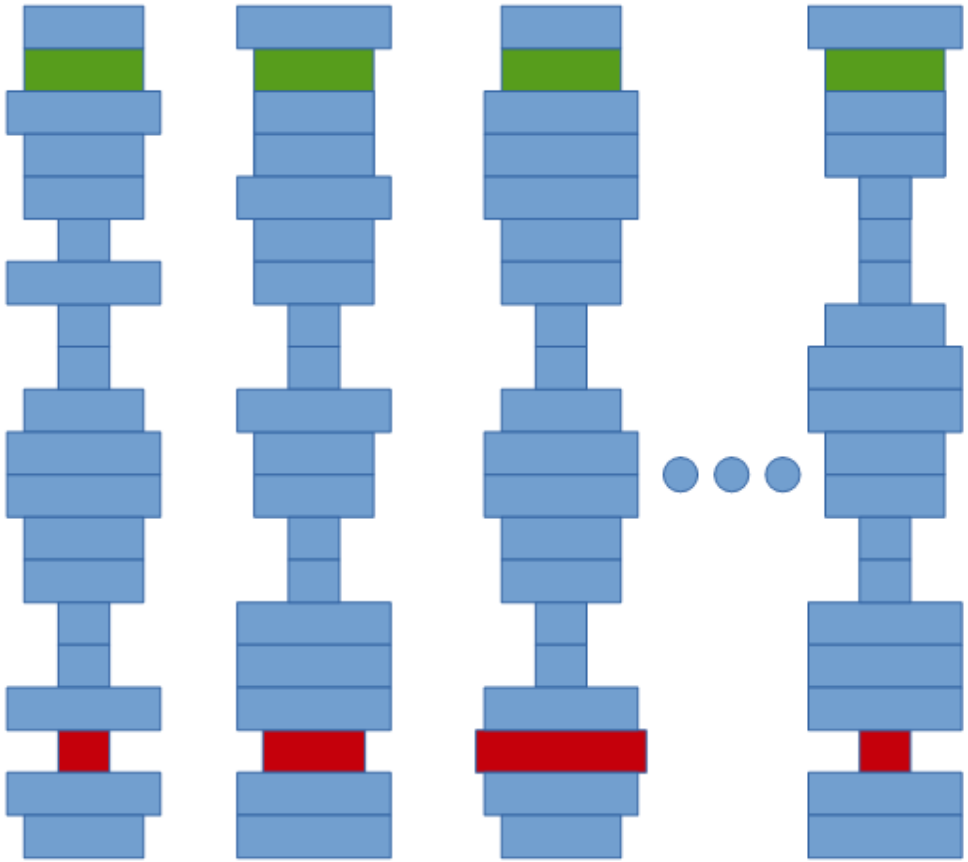


- The Patterns have a **Majority Logic**
- The Majority **Threshold** is **Programmable**
- If the Matches are more then the threshold

↓

Readout address

Variable Pattern resolution



- **Set** a different **resolution** for each CAM in the **Pattern.**
- Each **CAM** cells could use from **2** up to **6 don't care** bits (LSB).
- **Tune** cells **width** on the input source
- **Save** memory **space** when a lower resolution data is enough to identify the coincidence.

Some other Features

- IP from Silicon Creations:

  SerDes LVDS @ 2.4 Gbit/s

- **Input bandwidth** = 8 bus x 2.4 Gbit/s = **19.2 Gbit/s**
- **Output bandwidth** = **2.4 Gbit/s**
- Internal Logic Speed 100 MHz
- Power supply:

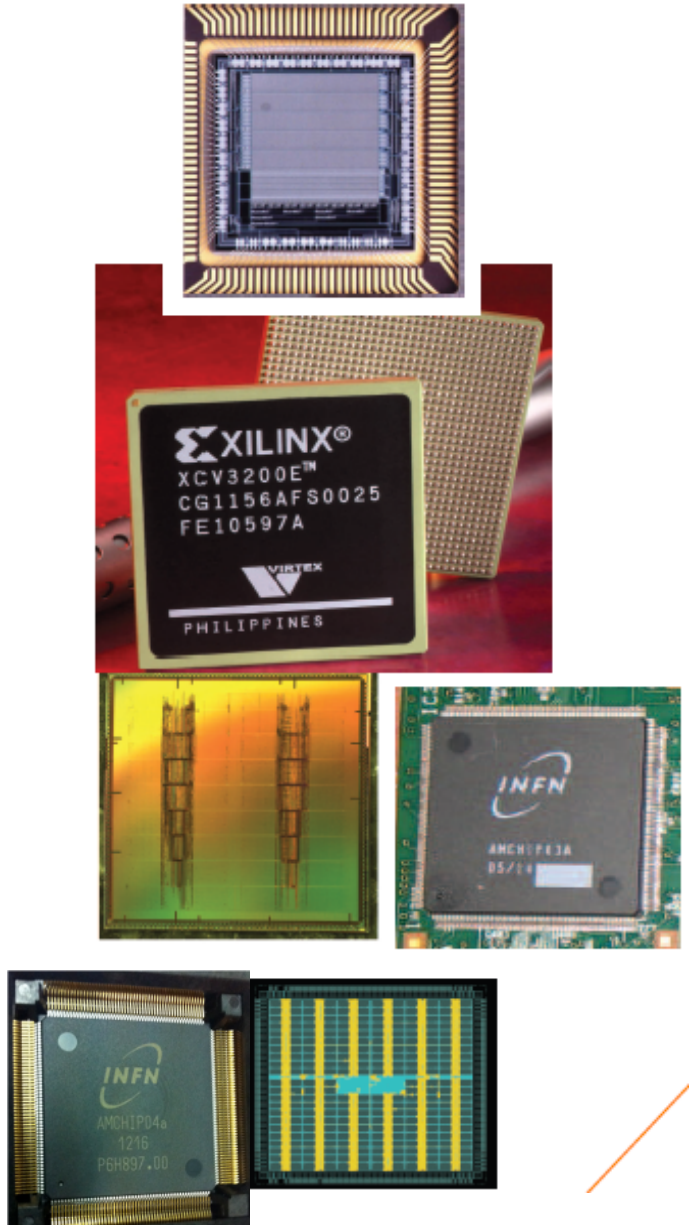
  2.5V I/O

  1.2V Std cell logic

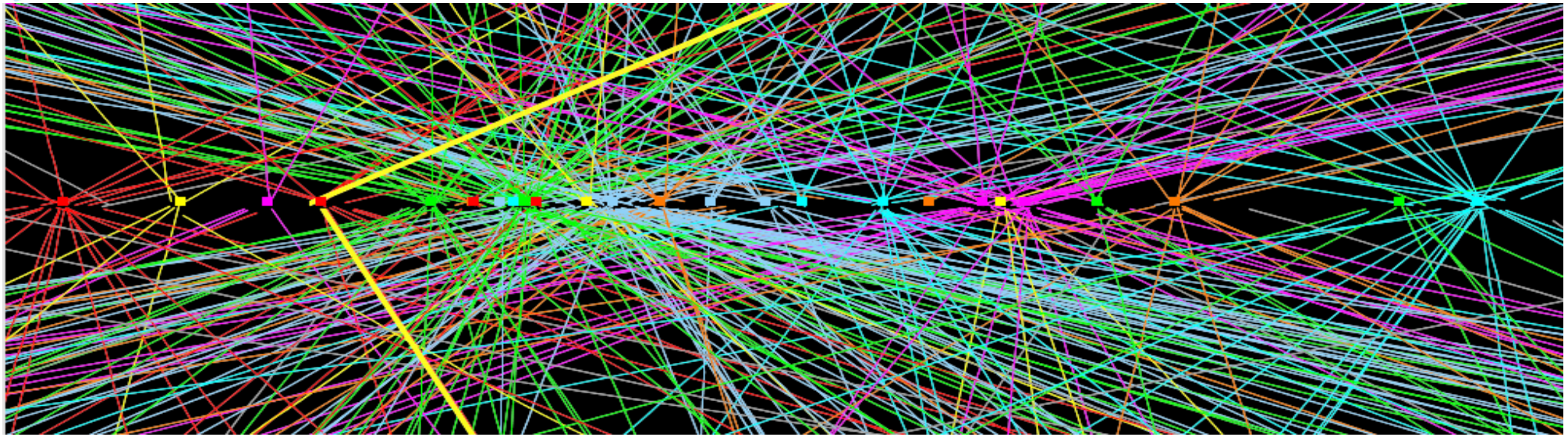
  1V Full Custom cell

- Total Power consumption 2.5W

- Final Package: HSBGA 529, 23 mm^2



High Energy Physic Applications



This is a product of two proton bunches collision; the Associative Memory does:

- Analyzes **thousand** of tracks in each event to decide in few microseconds which one are good enough to be stored.
- Solves the huge combinatory problem exploiting its parallelism.
- **Provides** a full list of high resolution tracks to High Level Trigger algorithms for each event.
- Event size: 1.5 Mbyte; event rate: 100kHz; Total system bandwidth 150 Gbyte/s

Applications outside of HEP:

- AM chip in the low level
- AM chip in the high level

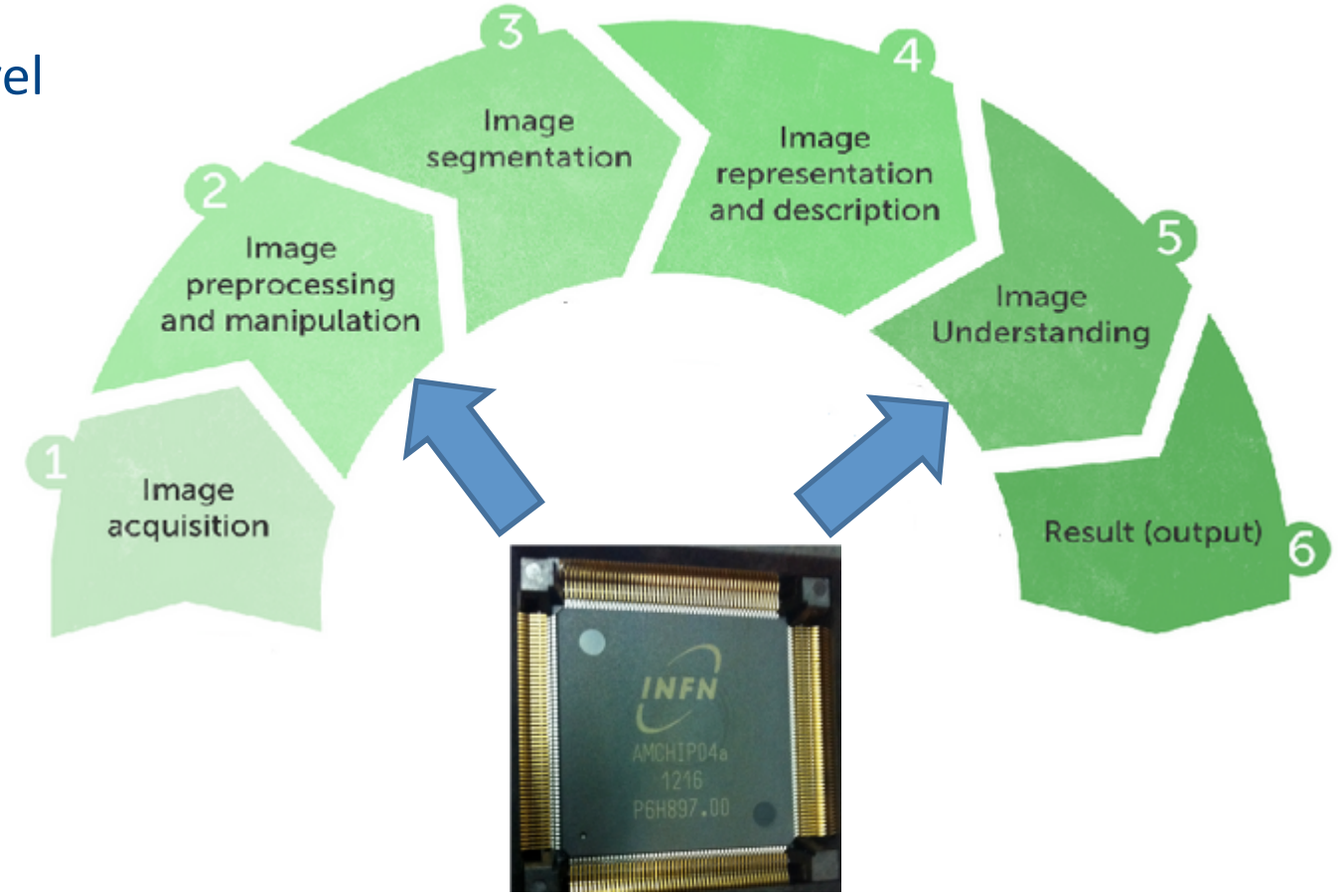
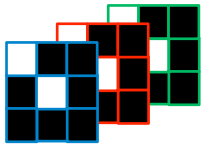
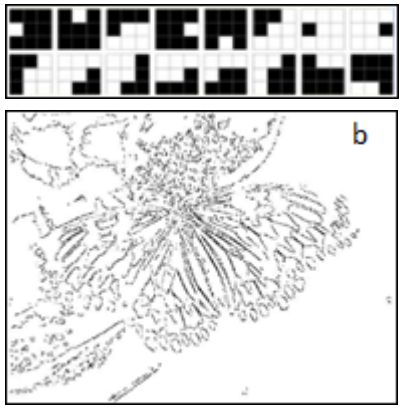


Image pre-filter: Michela Del Viva algorithm (previous talk)

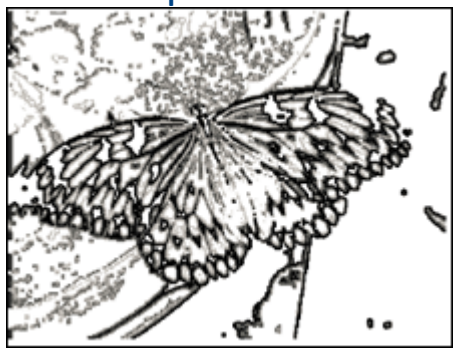
- Store in the memory the significant patterns (Es. 3x3) to recognize the image.
- B/W  2^9=512 patterns
- B/W + time  2^{27}= 128 M patterns
- Reconstruct the image accepting only patterns that match the stored ones
- The result is a compressed image, where is possible to recognize the relevant features

Accepting only these 16 stored patterns:



4 grey level: 2000 stored patterns

1/64 di 1 chip = 50 mW



AM chip in the high level

- CAM based, high density and high mach rate
- Independence between input
- Majority Logic
- Don’t care bits
- High bandwidth

- We are studying the possibility to use this HW in the “Image Understanding” phase
  - Binary classification
  - Machine learning

Conclusion

- AM chip Hardware architecture
- Useful Features
- HEP Application
- Outside HEP Applications

Thank You!

Are there any questions?

Email: saverio.citraro@for.unipi.it

Backup

Variable Pattern resolution, Memory space

- The coincidence to be find:
  - 28,0°< T < 28,9° AND P =1010 mBar ecc. AND V=5 m/s
  - **Without** don't care bits I have to store:

    28,0° 1010 mBar 5 m/s …

    28,1° 1010 mBar 5 m/s …

    28,2° 1010 mBar 5 m/s …

    …

    28,9° 1010 mBar 5 m/s …

  - **With** don't care bits I can store:

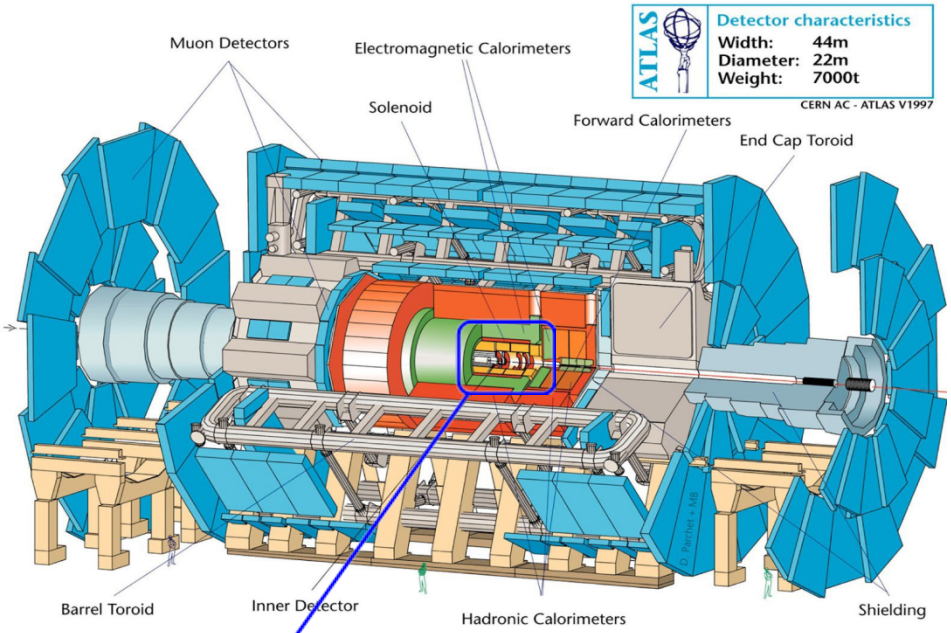
    28,X° 1010 mBar 5 m/s …

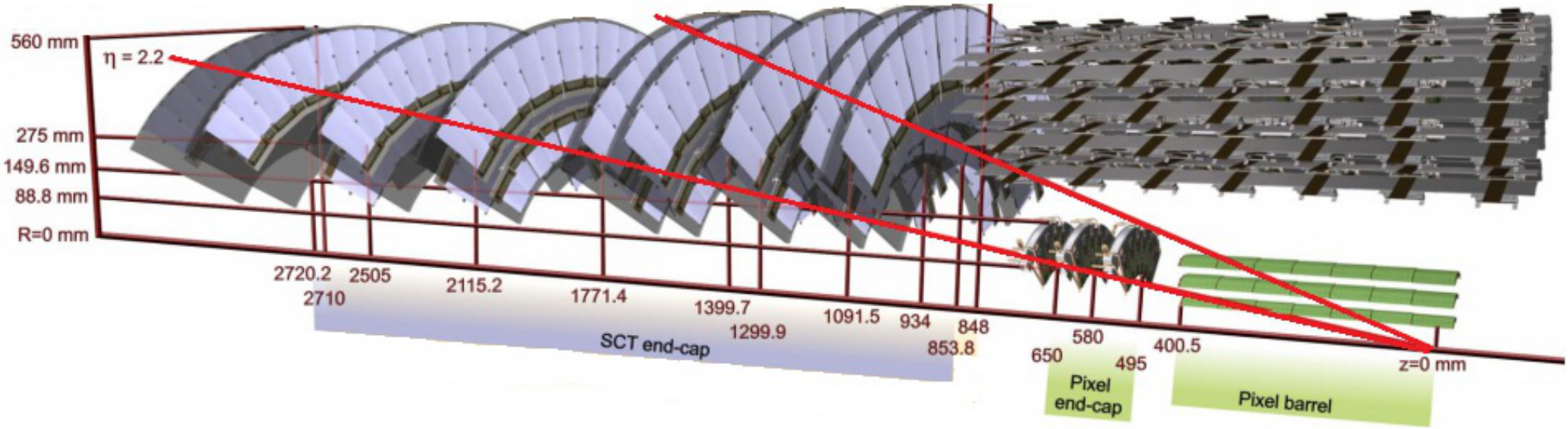
ATLAS silicon detector

- FTK reconstructs charged particles trajectories in the silicon detector (Pixel & SCT) at "1.5 trigger level".
- Extremely difficult task

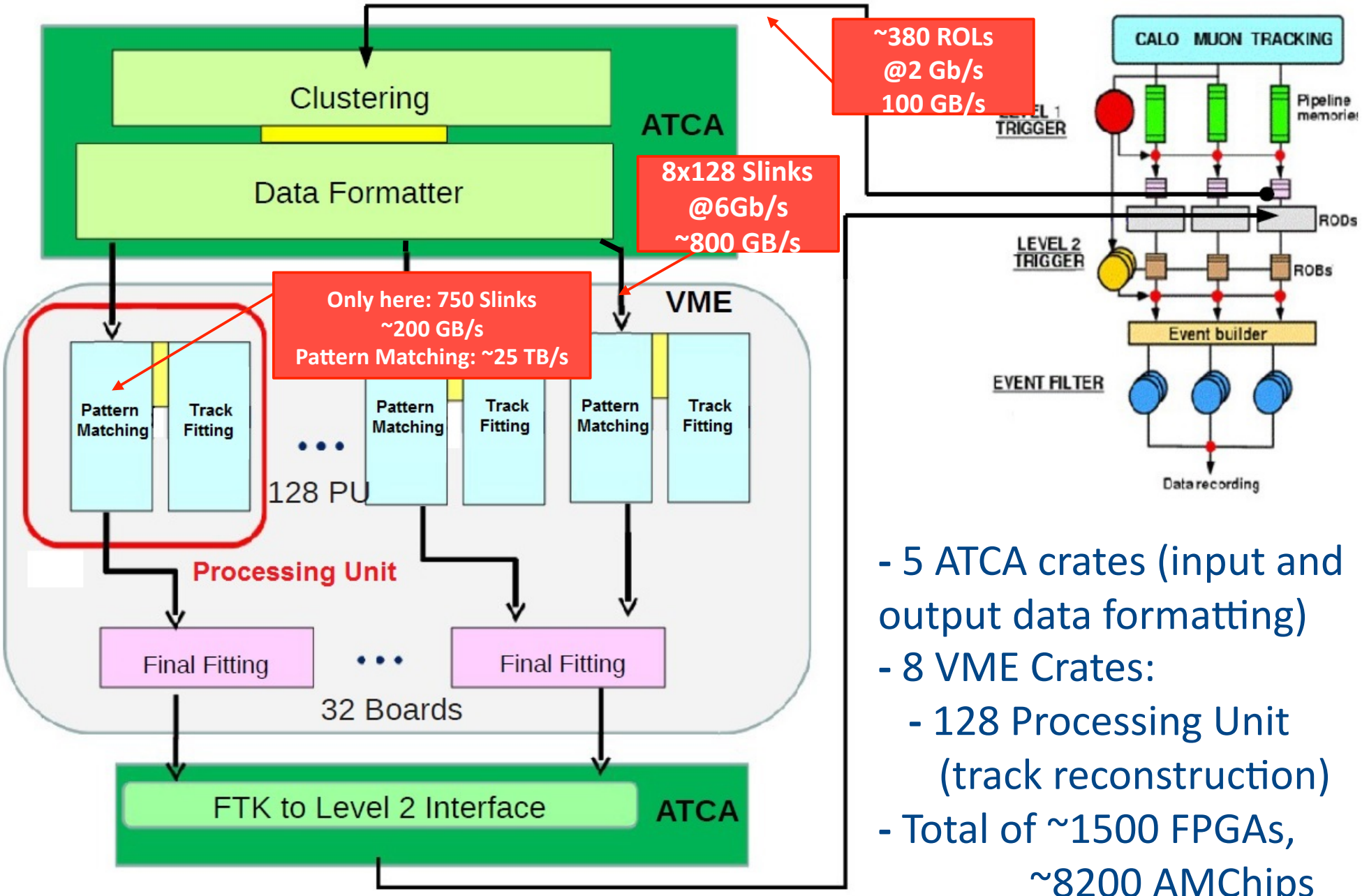
  100KHz processing rate

  ~70 overlapping events (pile-up) at highest luminosity.



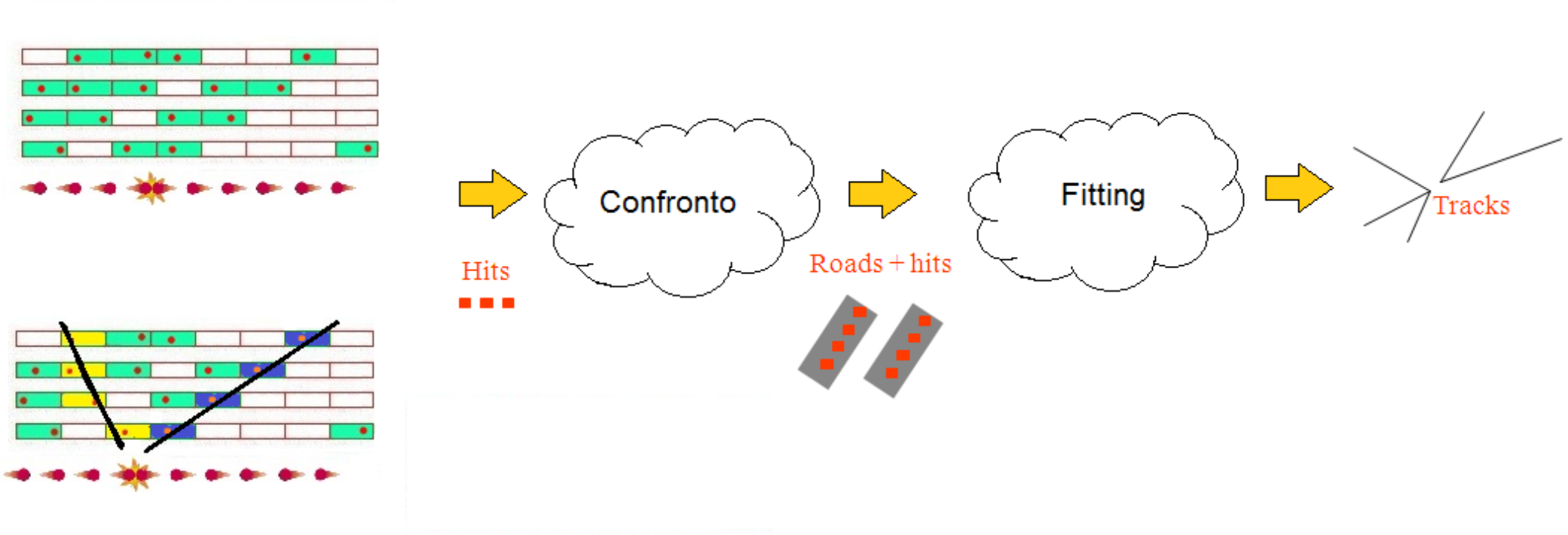


FTK Architecture



- 5 ATCA crates (input and output data formatting)
- 8 VME Crates:
  - 128 Processing Unit (track reconstruction)
- Total of ~1500 FPGAs, ~8200 AMChips

Pattern matching



- Pattern Bank: All the possible patterns (low resolution real track candidates) are precalculated and stored in the Pattern Bank.
- Pattern matching: All the hits in each event are compared with all the patterns in the Bank and track candidates (ROADs) are found.
- Track Fitting: Fits of the full resolution silicon HITs contained in each ROAD determine particle tracks parameters.

Processing Unit