The Associative Memory system for the FTK processor at ATLAS

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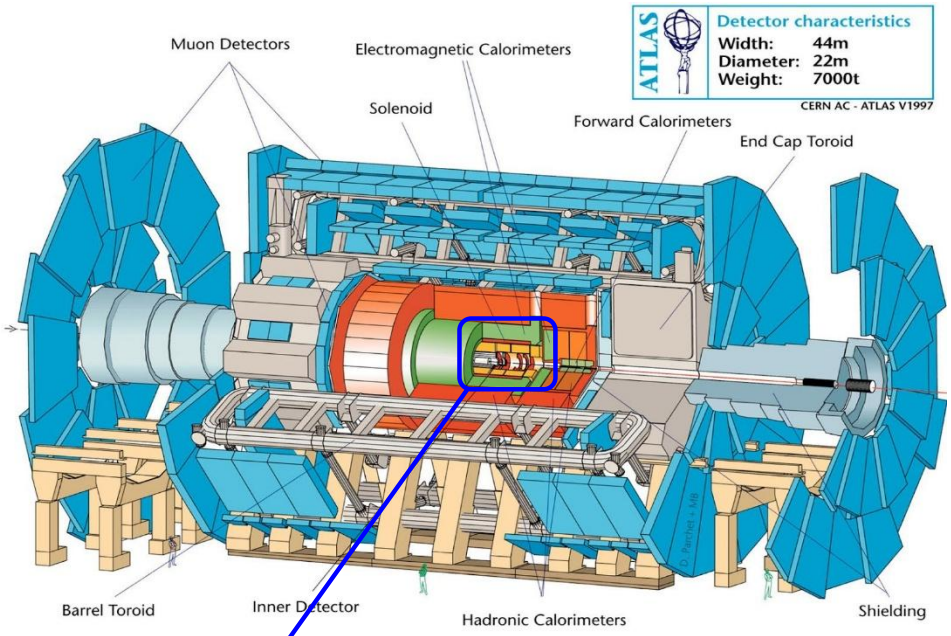
Outline

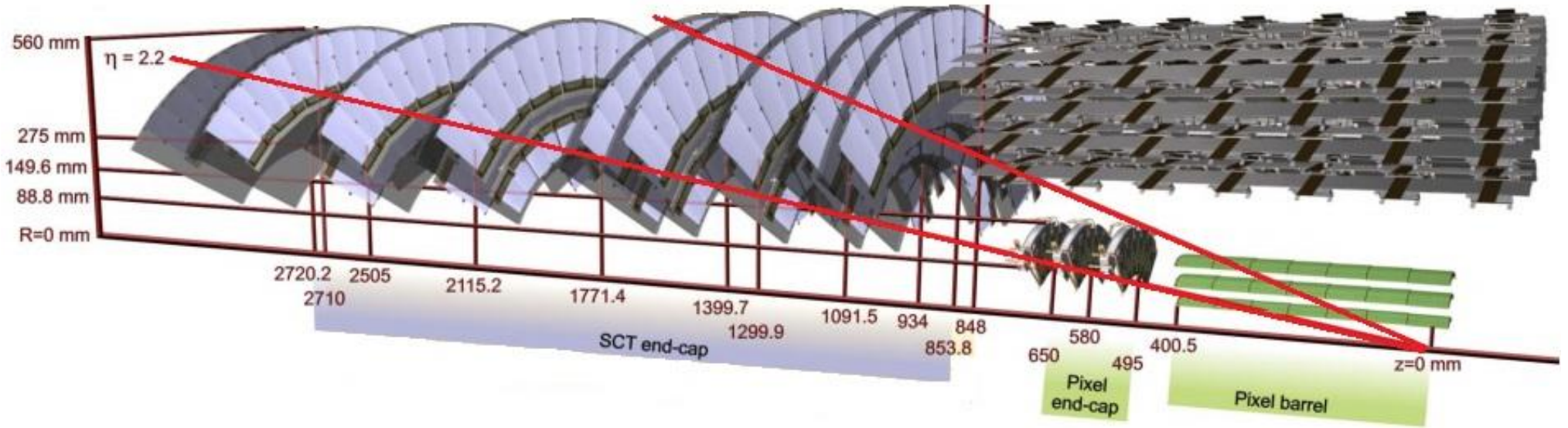
- Fast TracKer (FTK): On-line tracker for Atlas upgrade
- FTK architecture: description of the Associative Memory system
- Result of the prototypes testing
  - High speed links testing
  - Pattern Matching in the AM chip
  - Crate cooling test
- Evolution of the AM system
- Conclusion

An online silicon detector tracker for the ATLAS upgrade

- FTK reconstructs charged particles trajectories in the silicon detector (Pixel & SCT) at “1.5 trigger level”.
- Extremely difficult task 100kHz processing rate

  ~70 overlapping events (pile-up) at highest luminosity.





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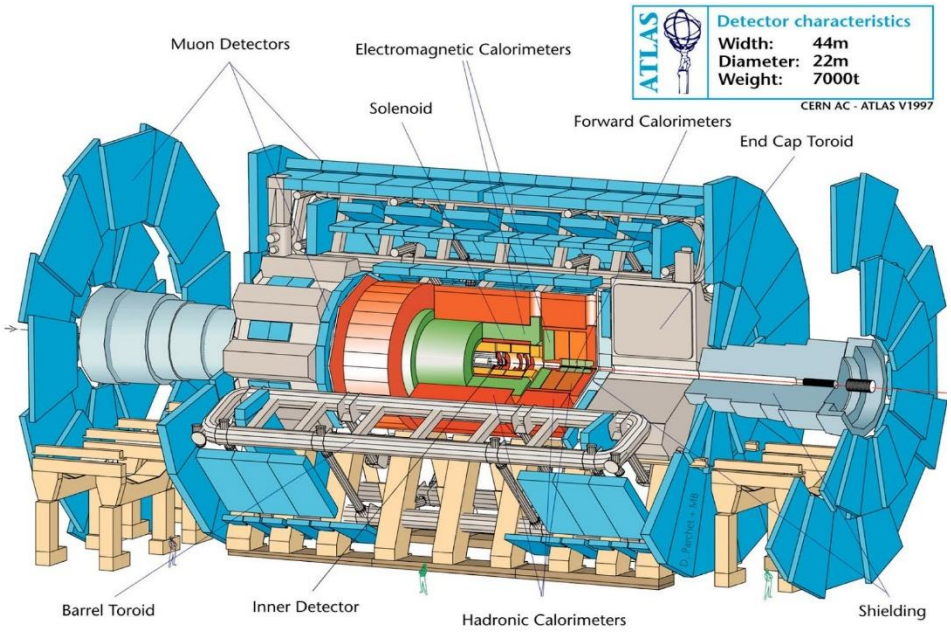
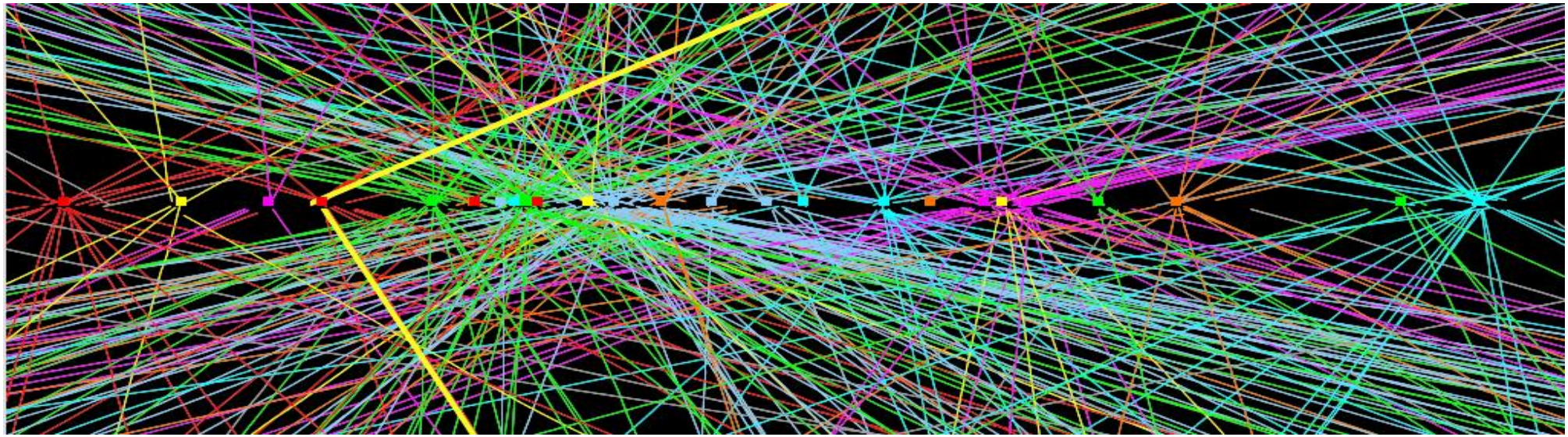
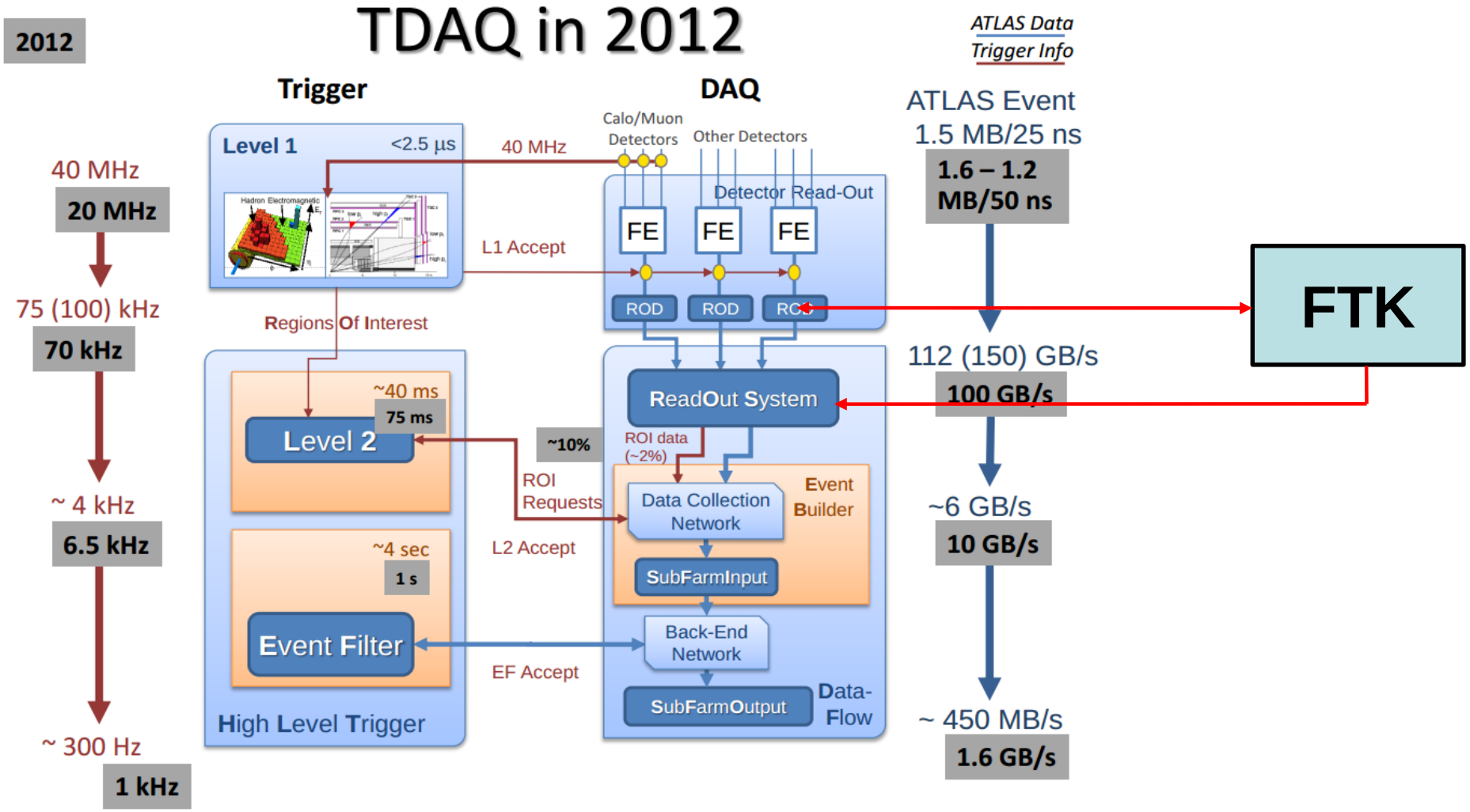


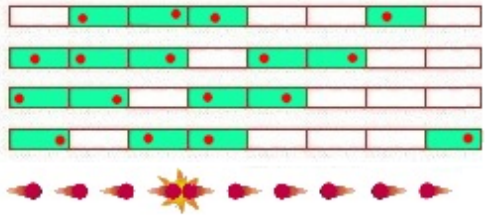


“1.5 Level Trigger processor”

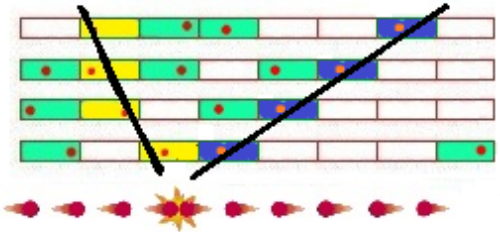


- Silicon data currently used only locally (ROI) and late in Level 2.
- FTK reconstructs all tracks with PT>1 GeV/c in time for Level 2.
- Track parameters are computed with full detector resolution.

FTK: Pattern matching & track fitting



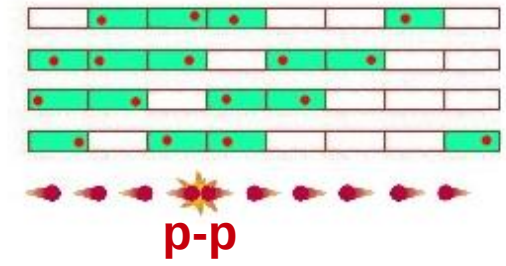
p-p



p-p

- **Pattern Bank**: All the possible patterns (low resolution real track candidates) are pre-calculated and stored in the Pattern Bank.

FTK: Pattern matching



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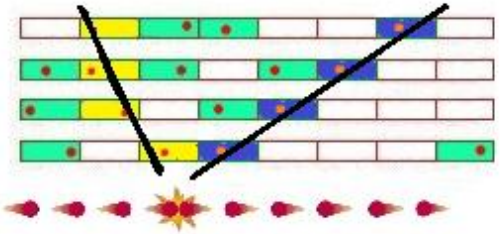

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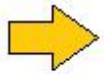
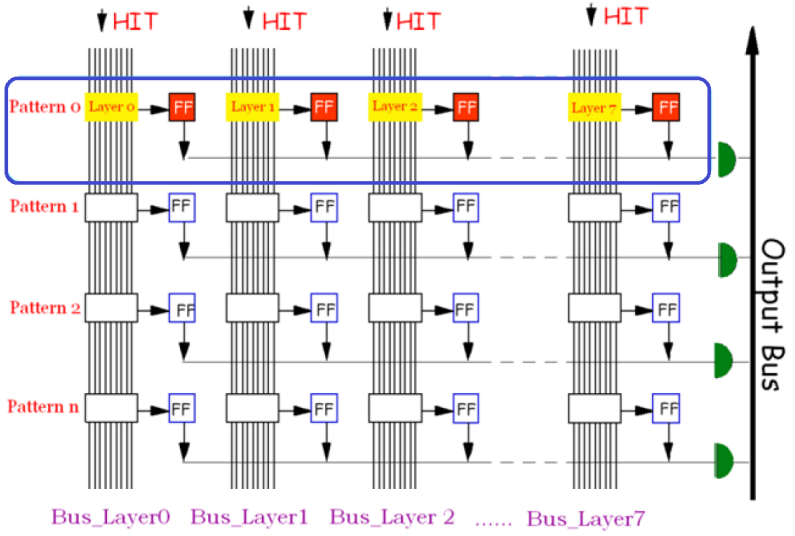


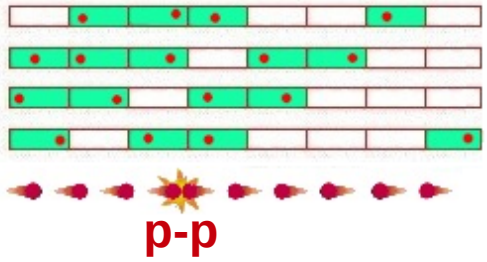
Hits

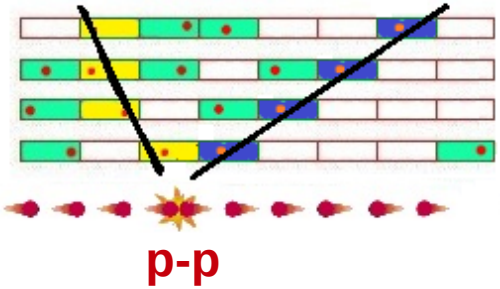


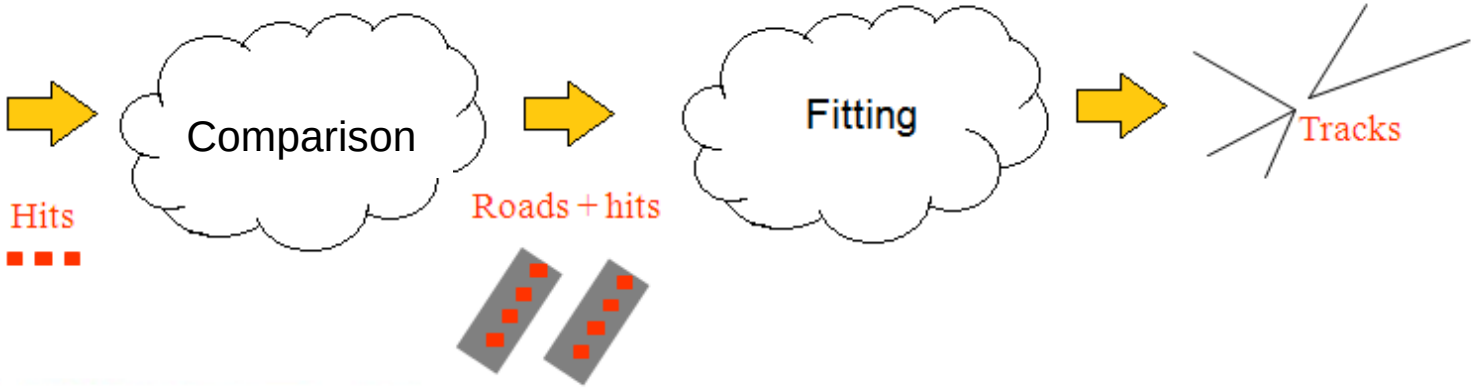
AMChip

- **Pattern Bank**: All the possible patterns (low resolution real track candidates) are pre-calculated and stored in the Pattern Bank.
- **Pattern matching**: All the hits in each event are compared with all the patterns in the Bank and track candidates (ROADs) are found.

FTK: Track Fitting



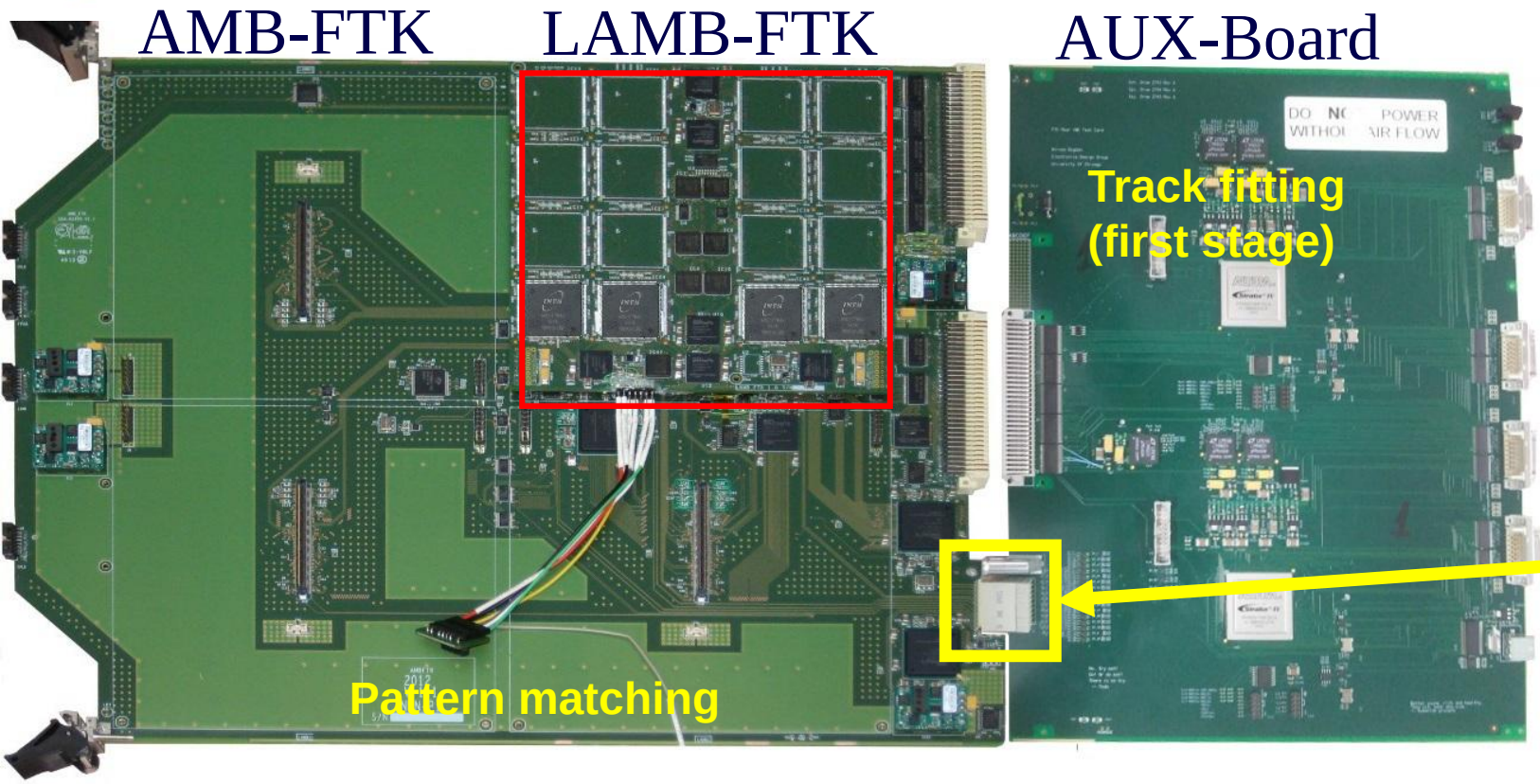




Road = Low resolution Track

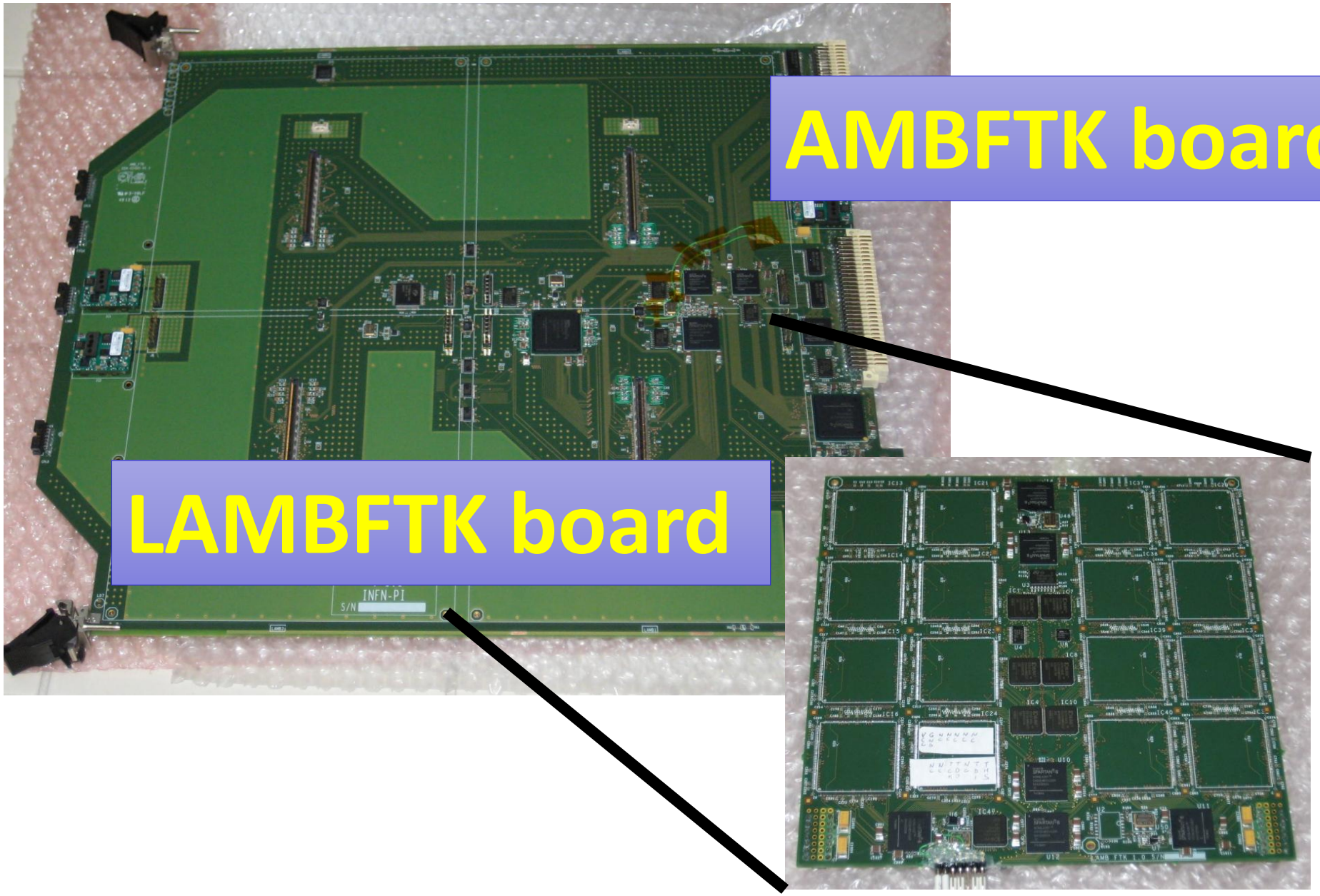
- **Pattern Bank**: All the possible patterns (low resolution real track candidates) are pre-calculated and stored in the Pattern Bank.
- **Pattern matching**: All the hits in each event are compared with all the patterns in the Bank and track candidates (ROADs) are found.
- **Track Fitting**: Fits of the full resolution silicon HITs contained in each ROAD determine particle tracks parameters.

FTK Processor Unit



- Processing Unit: 9U VME board (AMB-FTK) + large Rear card (AUX Card) + 4 little mezzanines (LAMB-FTK)
- Global processor is composed from 8 VME crate and 5 ACTA crate
- Silicon HITs relative to events accepted by Level 1 (~100kHz) are distributed to all AMChips.
- 1 HIT is compared with ~ 8x10^6 of Precalculated pattern.

AM System Logic



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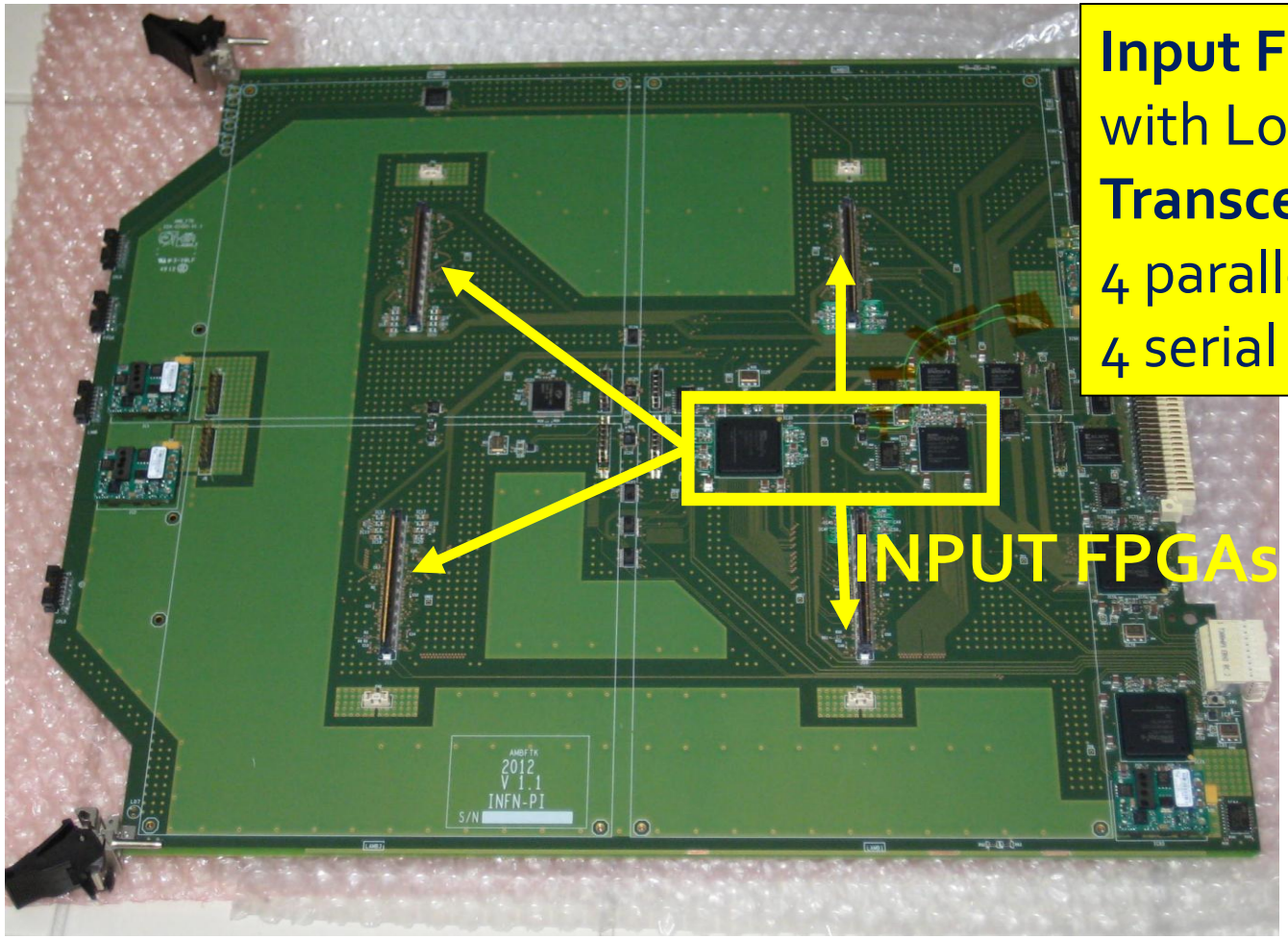
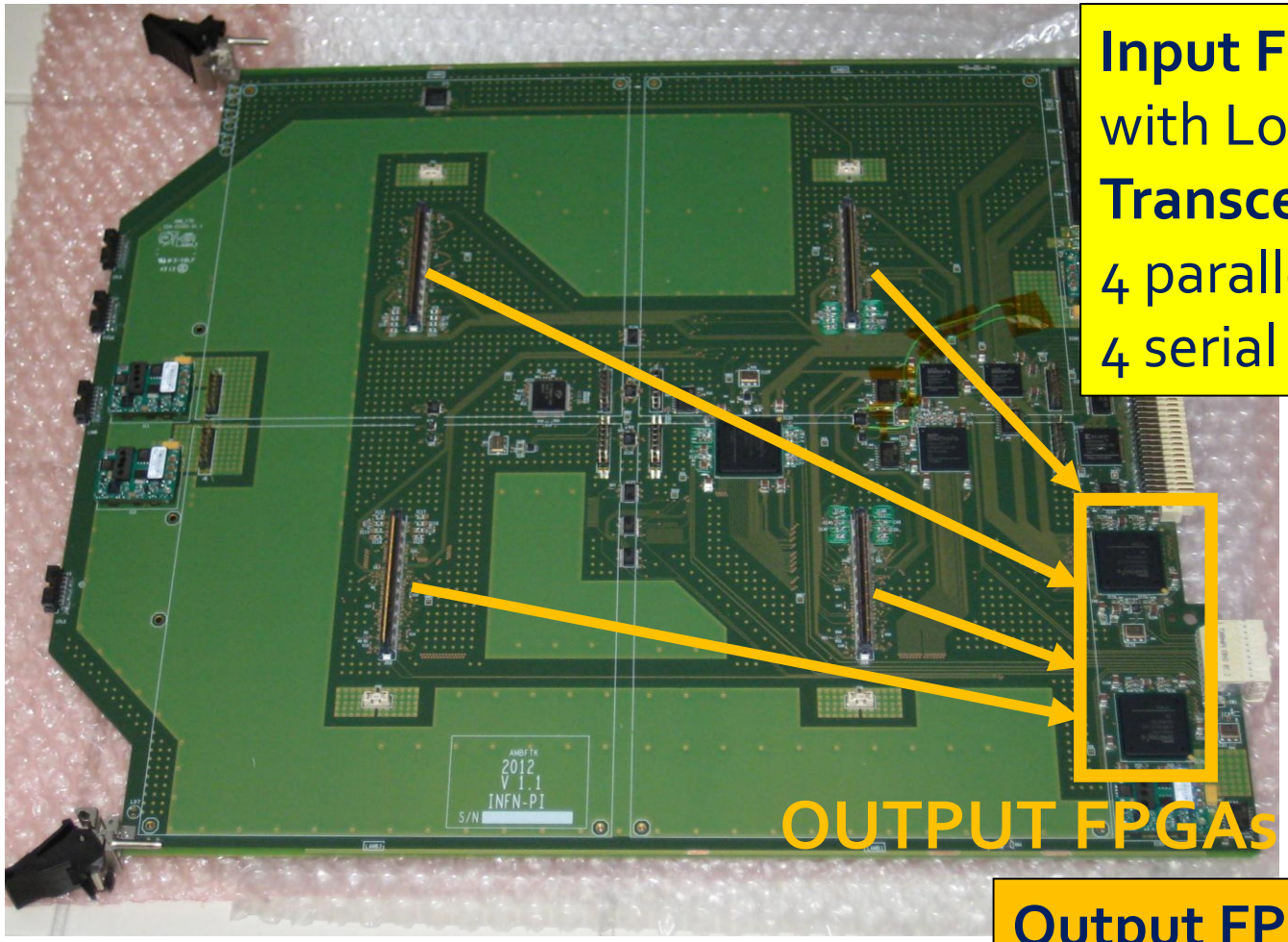


Input FPGAs: Xilinx Spartan6 with Low Power **Gigabit Transceiver (GTP)**
4 parallel buses @ 100MHz
4 serial buses @ 2Gbps

AM System Logic



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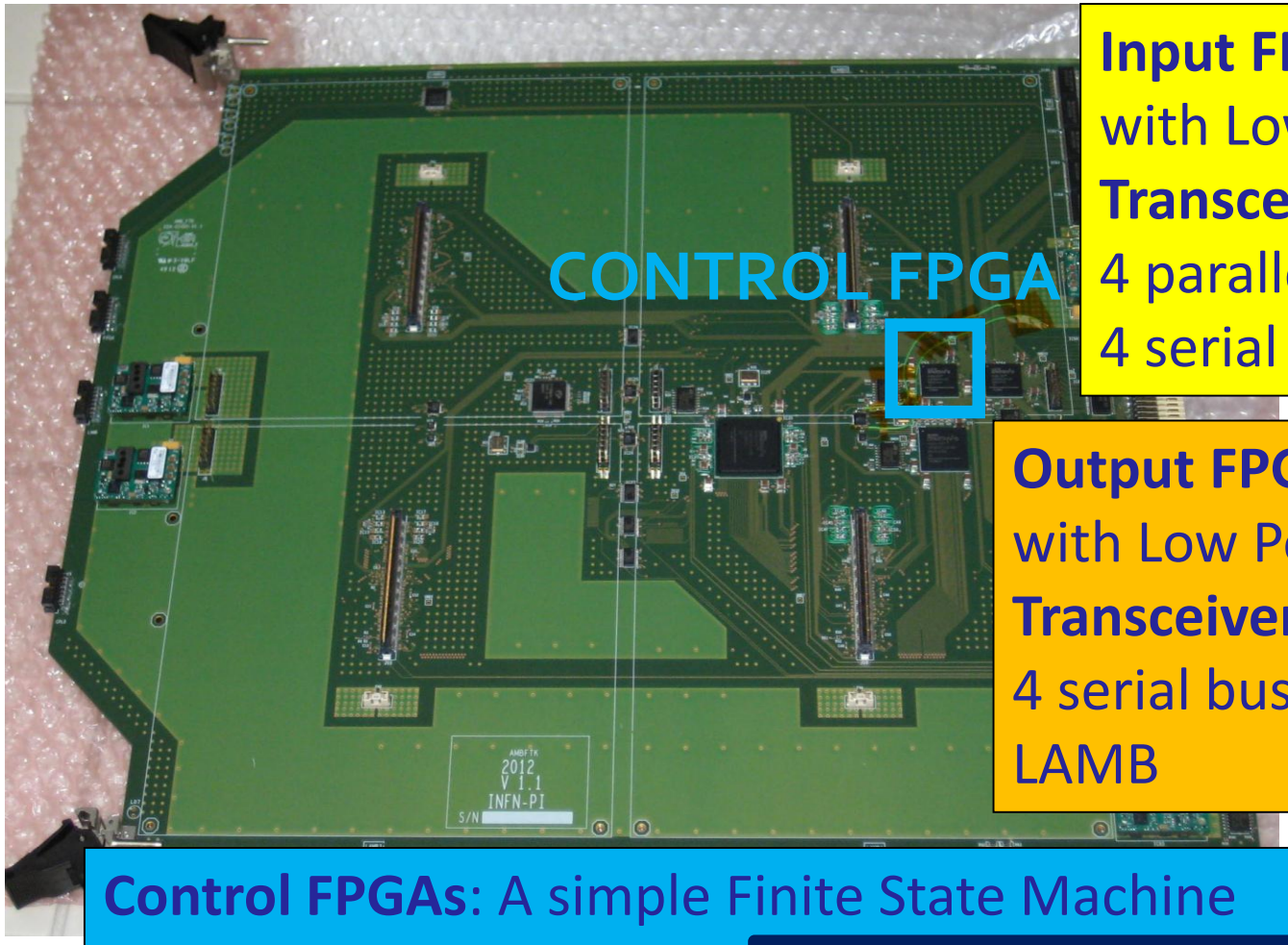
4 serial buses @ 2Gbps from each LAMB

AM System Logic



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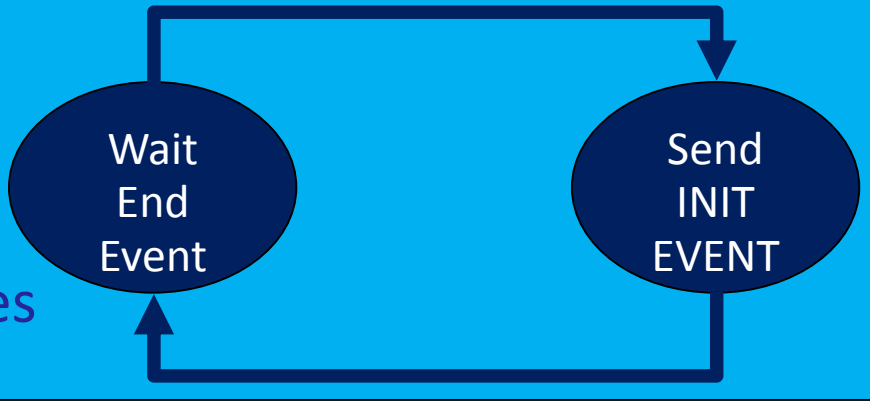
4 serial buses @ 2Gbps

Output FPGAs: Xilinx Spartan6 with Low Power **Gigabit Transceiver (GTP)**
4 serial buses @ 2Gbps from each LAMB

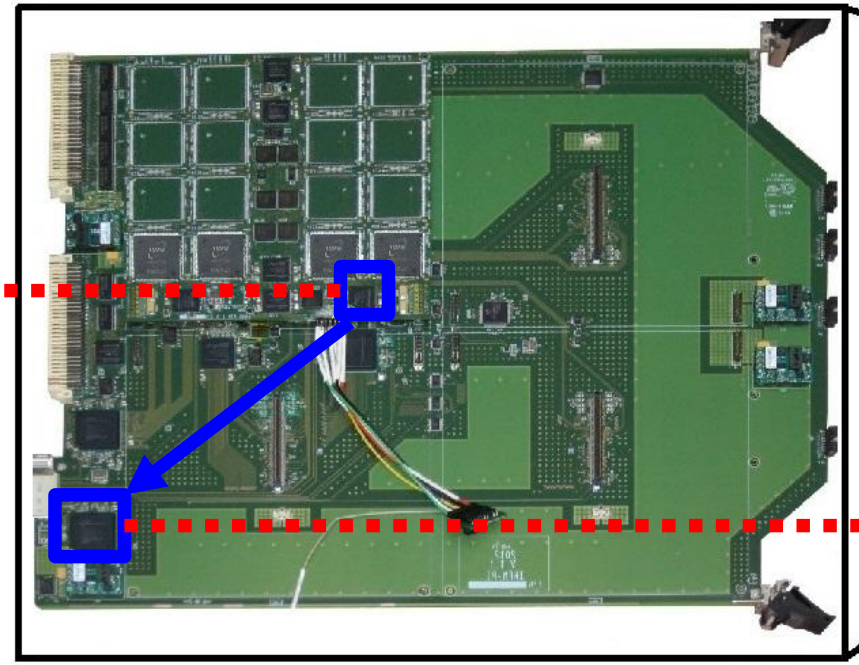
Control FPGAs: A simple Finite State Machine

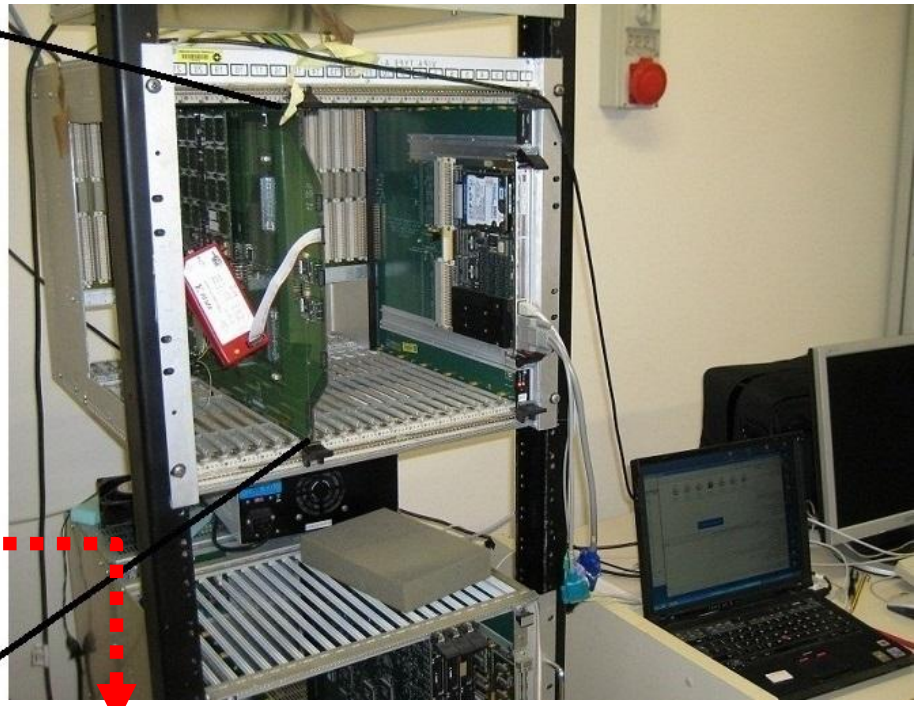
Wait for all End Event from input HIT buses and output ROAD buses



Initialization of the AMChip to receive the next event

Serial Link Test: Hit input and Road Output

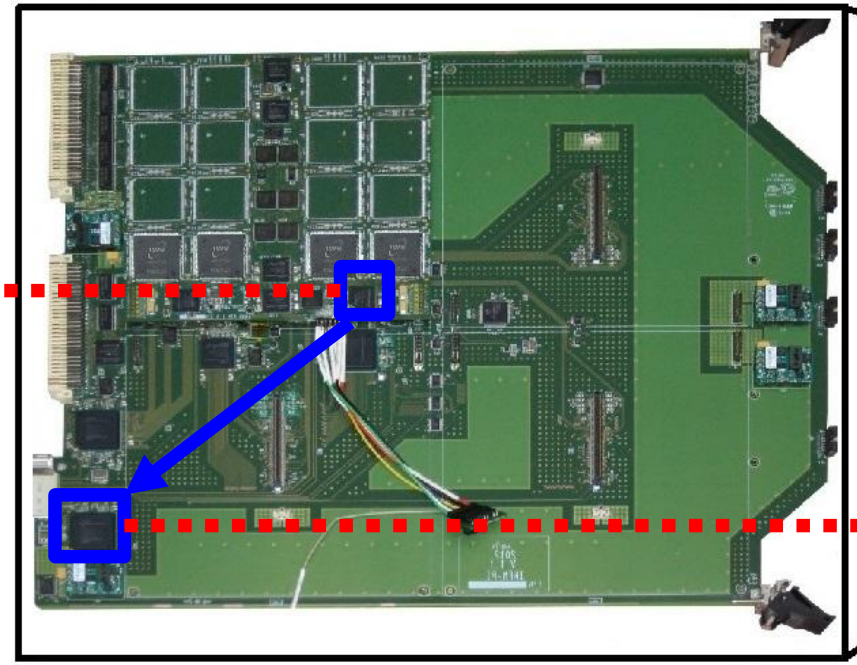


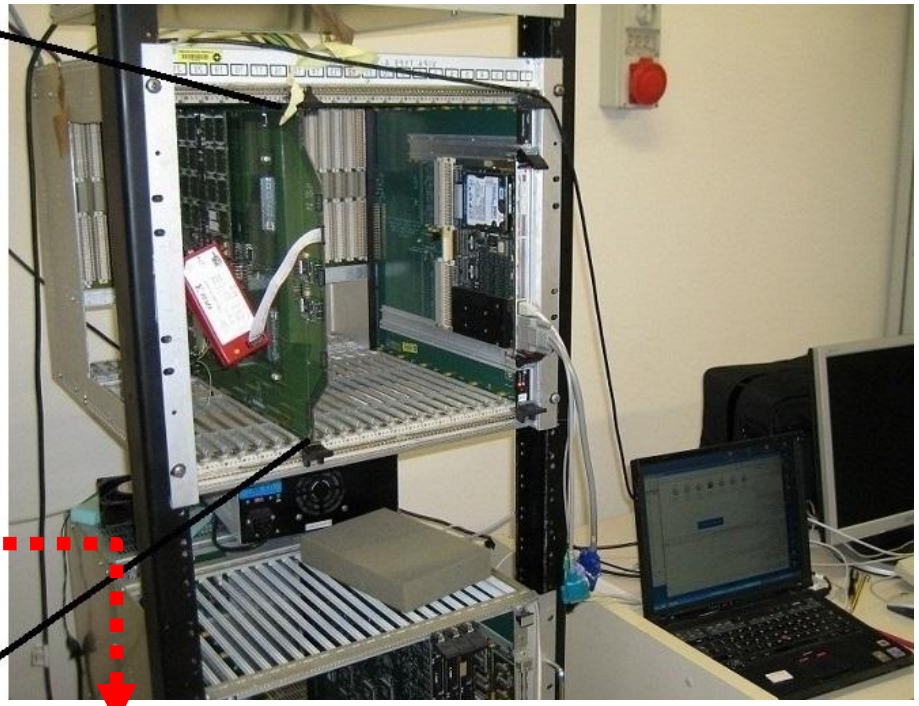


The serial link characterization and testing

- Simulation of the line with the SigXplore Cadence
- Evaluation of the quality of the link with Pseudo Random Bit Sequence (PRBS)

Serial Link Test: Hit input and Road Output





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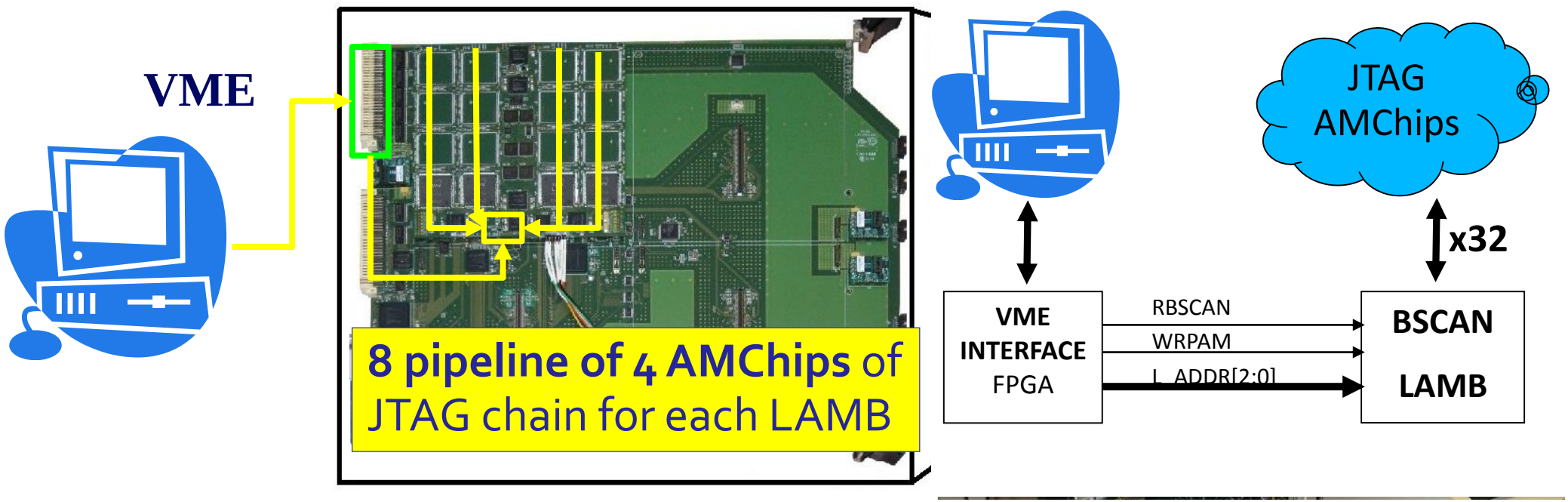
Bit Error Rate

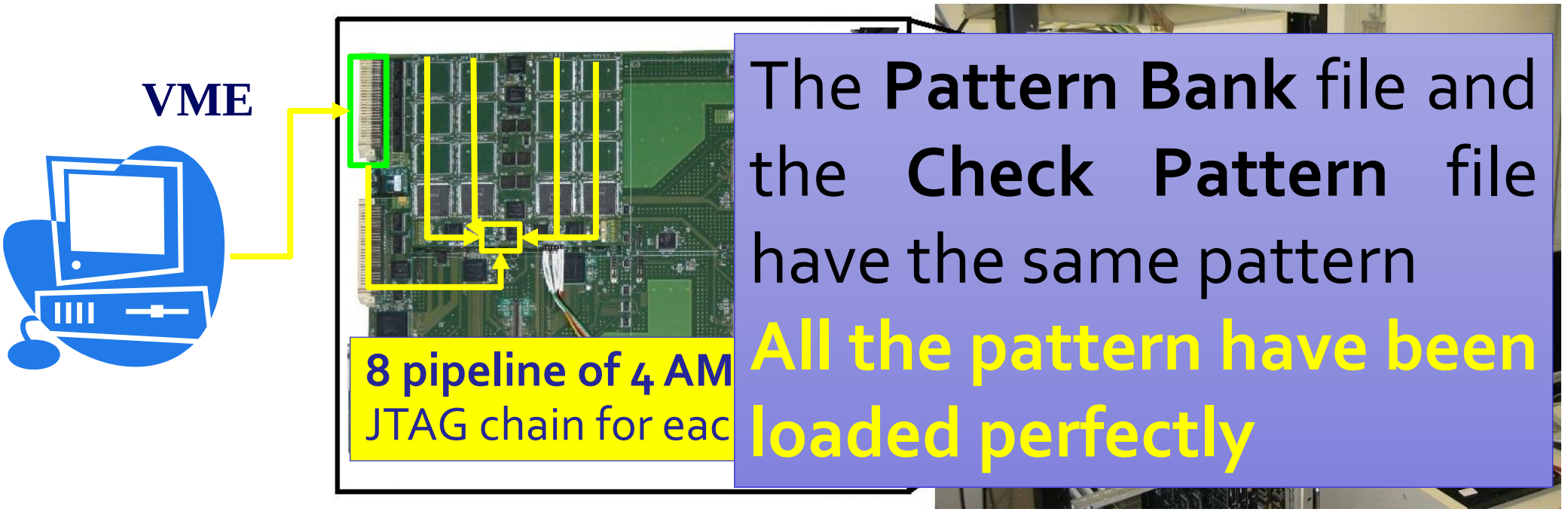
BER< 10^{-10}

AMChips configuration



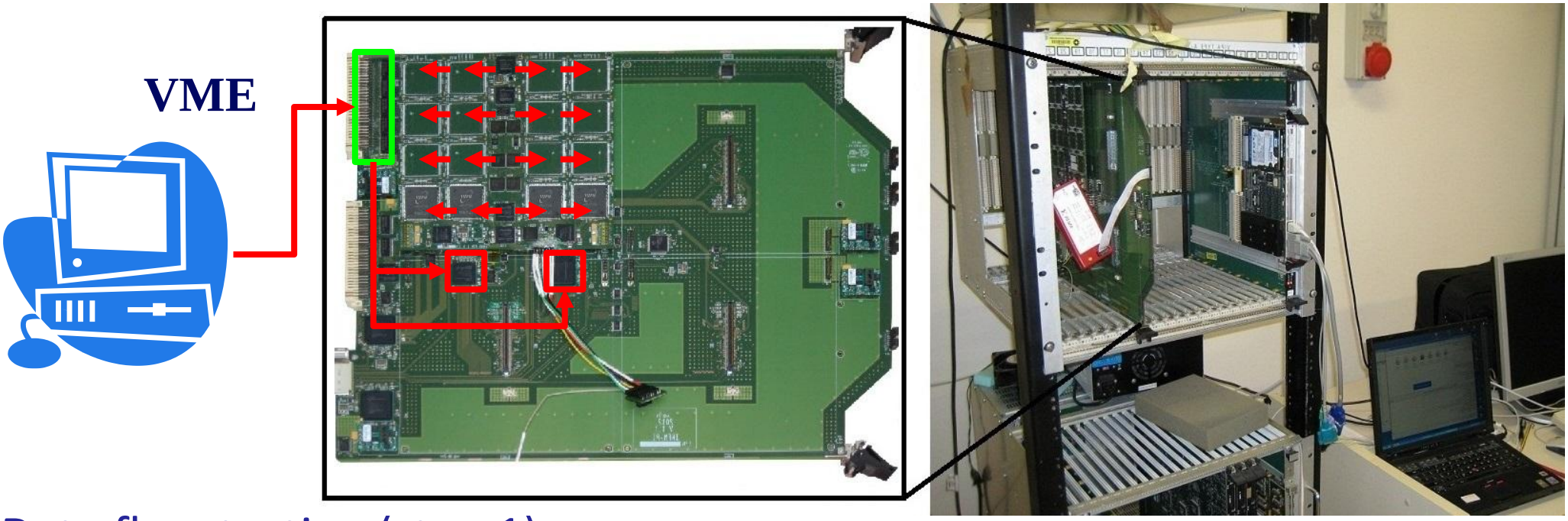
- The AMChip are accessible via JTAG protocol => a dedicated FPGA perform the VME-JTAG conversion
- The JTAG controller of the all AMChips is controlled in parallel with several VME access.

AMChips configuration



- The AMChip are accessible via JTAG protocol => a dedicated FPGA perform the VME-JTAG conversion
- The JTAG controller of the all AMChips is controlled in parallel with several VME access.
- The simulated pattern bank is loading in all AMChips => a check pattern operation to show the successful of pattern loading

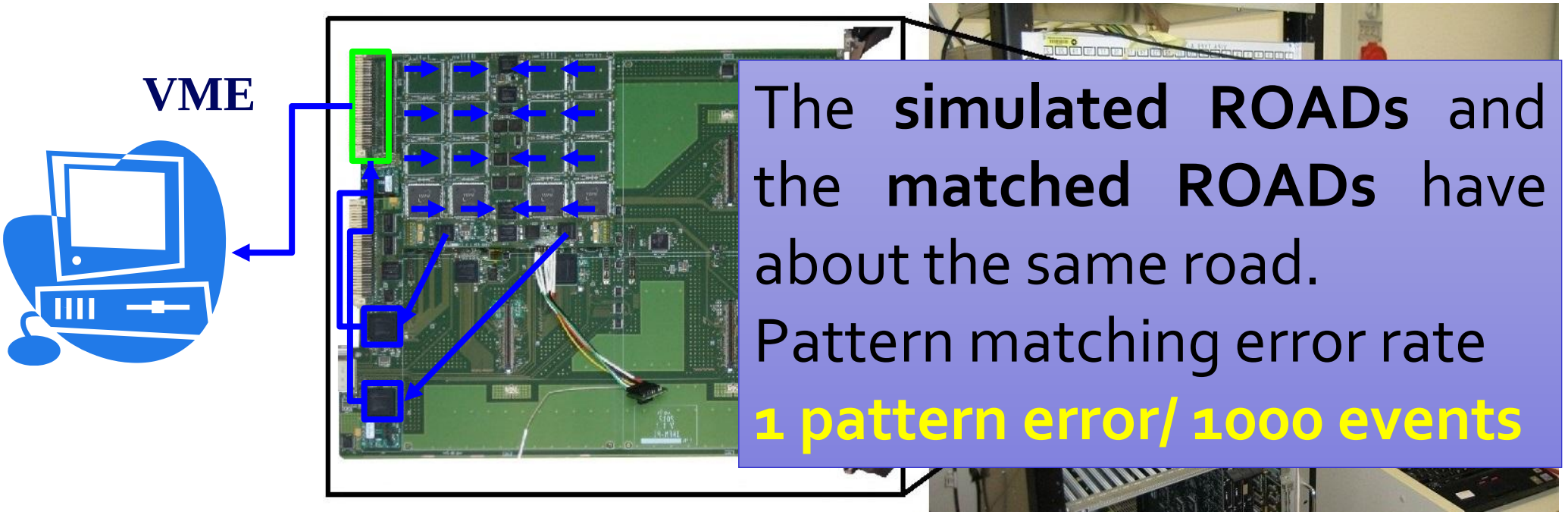
Data flow testing: input HIT distribution



Data flow testing (step 1)

- Simulate silicon HITS Input to generate a file
- Silicon HITS Input are loaded into the inputs FPGAs memory (red square) through VME.
- When the memory are all loaded, the FPGAs transmit data to he LAMBs at full speed.

Data flow testing: output ROADS collection



The **simulated ROADs** and the **matched ROADs** have about the same road.
Pattern matching error rate
1 pattern error/ 1000 events

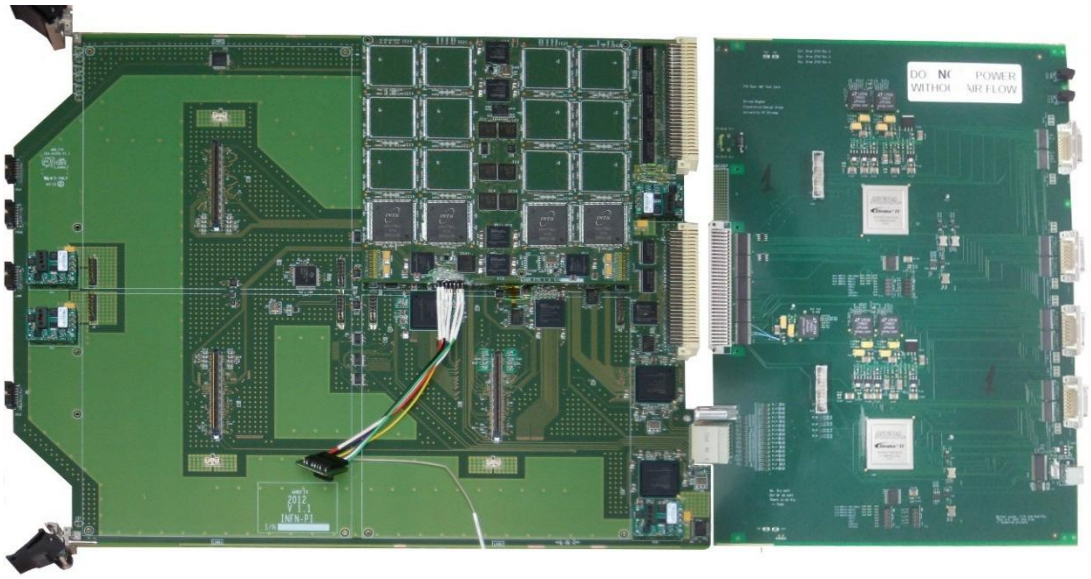
Data flow testing (step 2)

- After the all HITS is received from the all AMChips we send and INIT EVENT signal so the matched road can go out
- The road at full speed is Collected in the Output FPGAs (blue squares)

Data flow testing (step 3)

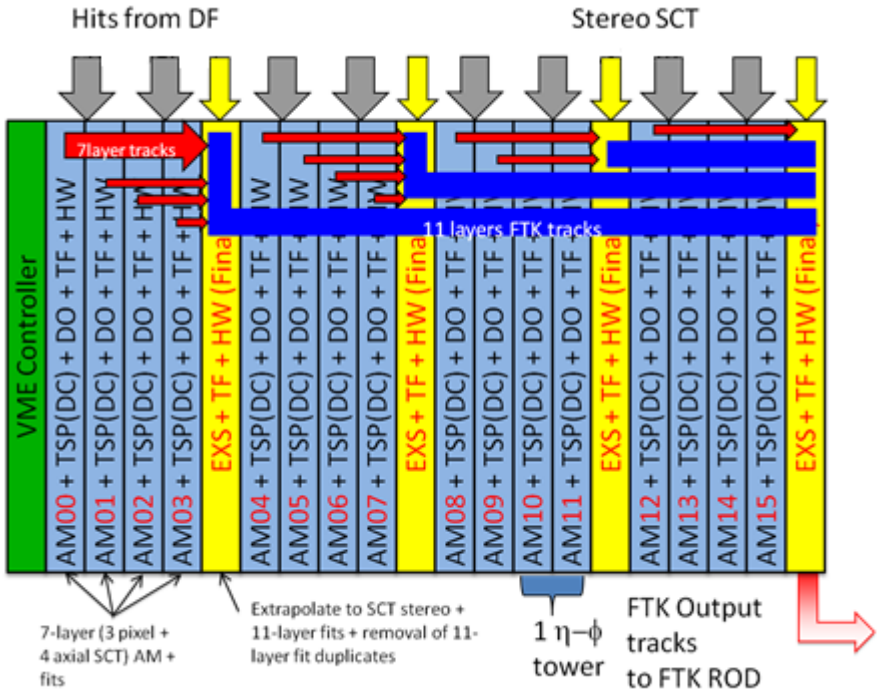
- The road is stored in memories that are read from VME and saved in a file
- Compare Hardware and Simulation output files

Cooling Tests



Power supply voltages for the FTK system:

- 5V
- 3,3V
- 1,2V

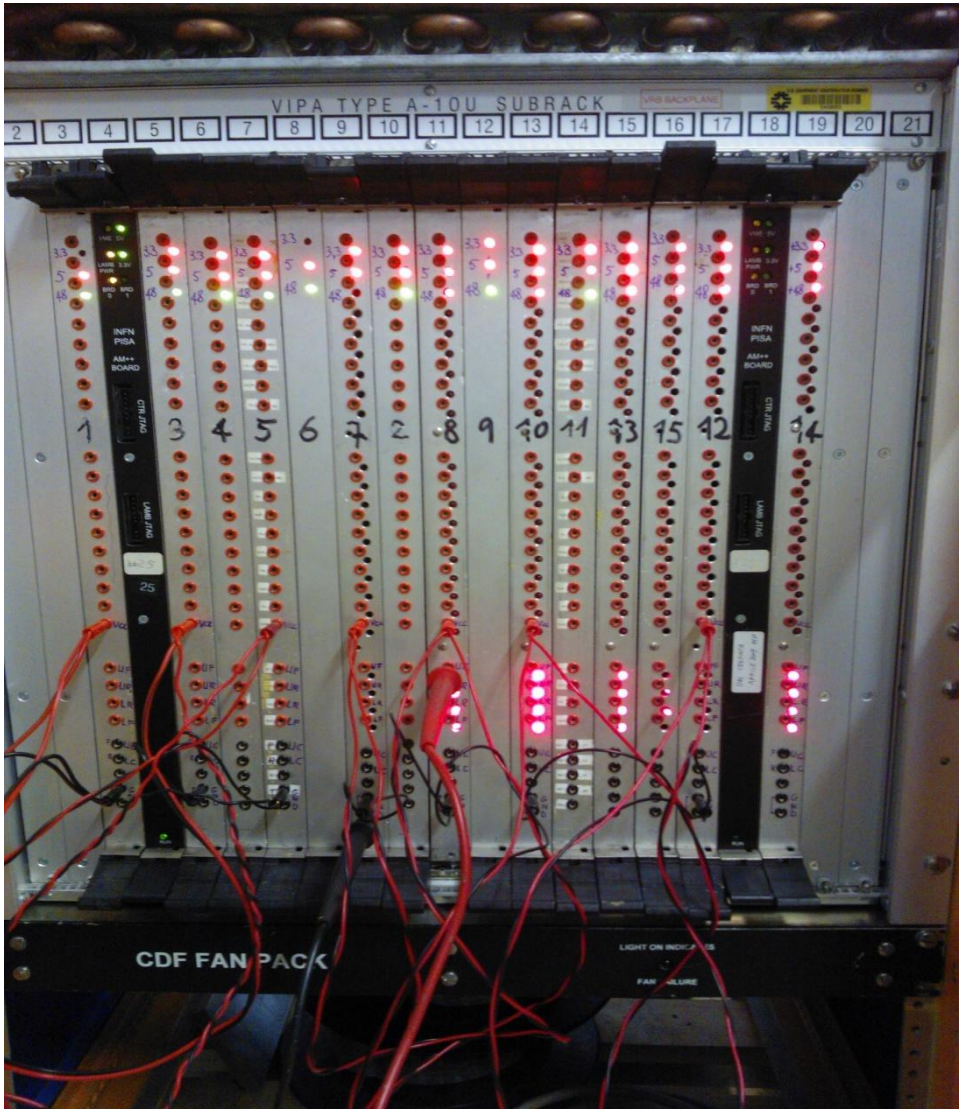


Expected power consumption

- 1 Processing unit ~ 300 W
- 16 PUs in a single VME crate
- ~ 5 kW per crate.

Need Cooling test!

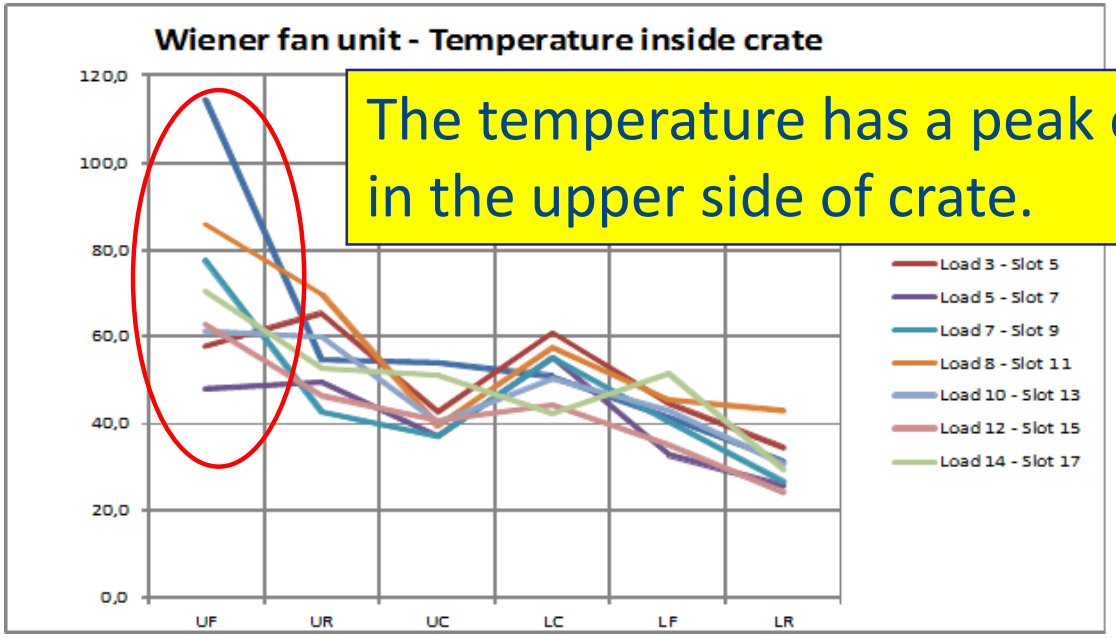
Cooling Tests without chiller



- Cooling test currently in progress INFN PAVIA.
- Power consumption simulated with resistors.
- Six sensor used to measure the temperature in the crate (red circles)

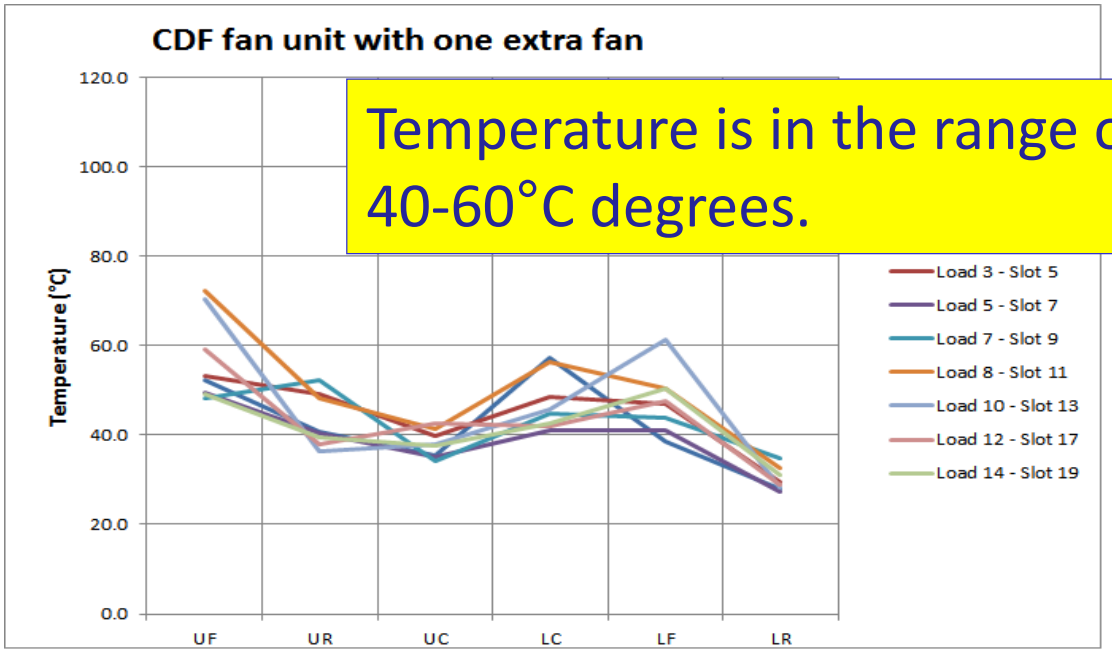
WEINER and CDF fan result

WEINER fan unit



The temperature has a peak of in the upper side of crate.

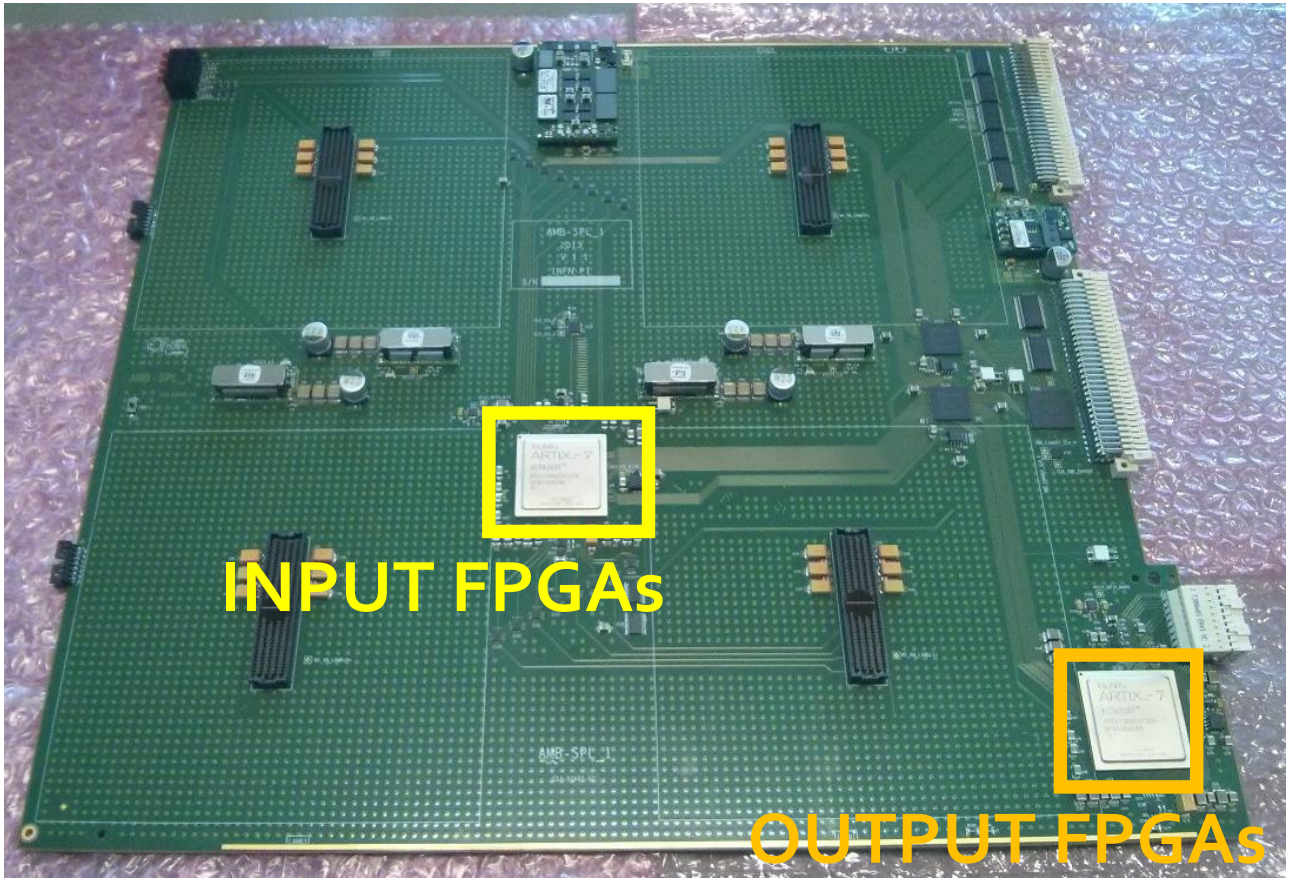
CDF fan unit



Temperature is in the range of 40-60°C degrees.

Evolution of the AM system

Evolution of the AMBoard: AMBSLP processor



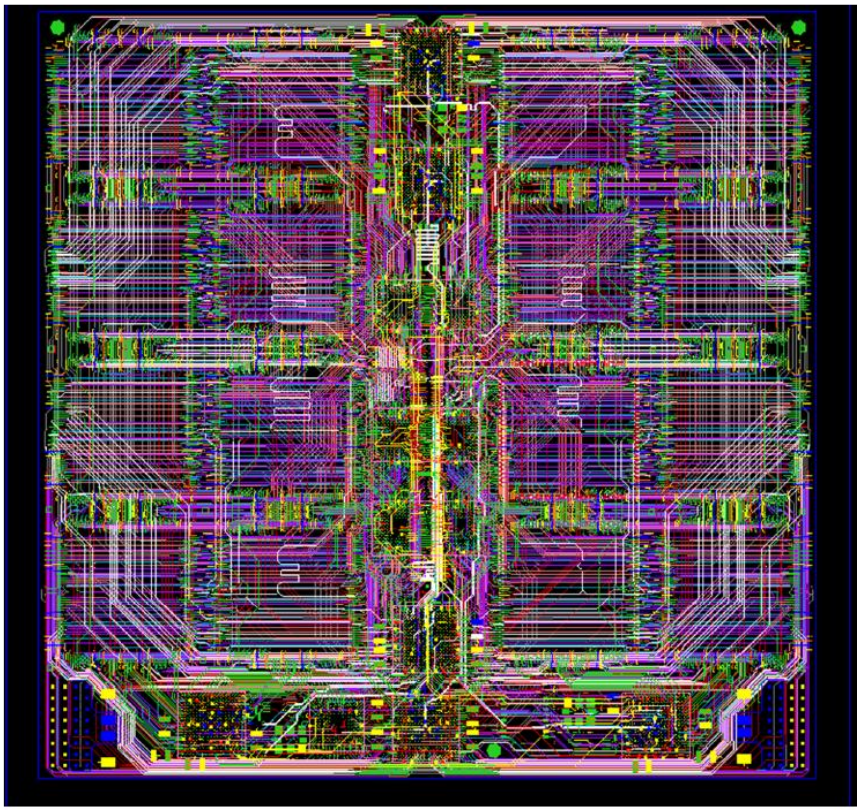
No parallel buses for HIT distribution

Only serial links connection

- **12 links** for the HITs @ **2Gbps**
- **16 links** for the ROADs @ **2Gbps**

Evolution of the AM system

Evolution of the mezzanine LAMB: LAMBSLP

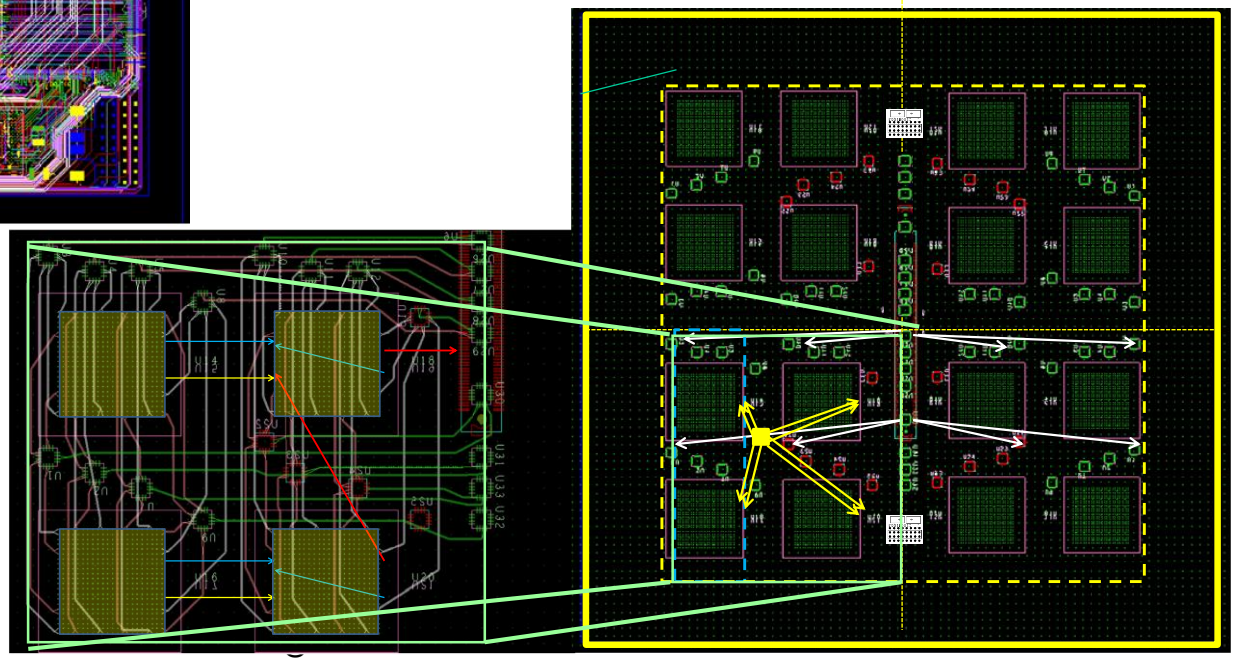


Old LAMB problem:

- **high density** of connection
- **high number of devices** for fan-out

New LAMBSLP:

- **Simplified routing**
- LAMBSLP **reduced size no FPGAs**



Conclusion

- We have described the **FTK processing unit** referring in particular to the **AM system for the pattern matching function**
- We have shown the result of the tests of the AM system
  - The **serial link connections** are very good quality for the 2Gbps rate
  - The results of the **pattern matching test** show that all complete system works very well.
- We have show **the cooling test** with the power consumption of the finale system
- We have described the evolution of the AM system with only serial link connections (**AMBSLP**)
  - All the previous tests have to be perform also for this one system

Thank You!